

Research Article

Quantization Effects on Period Doubling Route to Chaos in a ZAD-Controlled Buck Converter

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The quantization effect in transitions to chaos and periodic orbits is analyzed in this paper through a specific application, the zero-average-dynamics- (ZAD-) controlled buck power converter. Several papers have studied the quantization effects in the one periodic orbit and some authors have given guidelines to design digitally controlled power converter avoiding limit cycles. On the other hand many studies have been devoted to analyze the ZAD-controlled buck power converter, but these past studies did not include hardware considerations. In this paper, analog-to-digital conversion process is explicitly introduced in the modeling stage. As the feedback gain is varied, the dynamic behavior depending on the analog-to-digital converter resolution is numerically analyzed. Particularly, it is observed that including the quantizer in the model carries out several changes in the transitions to chaos, which include interruption of band-merging process by cascades of periodic inclusions, disappearing of band transitions, and multiple coexisting of periodic orbits. Many of these phenomena have not been reported as a consequence of the quantization effects.

1. Introduction

In the recent years, many physical systems have been modelled using the theory of non-smooth dynamical systems (NSDSs) [1]. The piecewise smooth dynamical system (PWS) approach has mainly been used to model nonsmooth phenomena such as switching, saturation, sliding, or impacting events [2, 3]. A good compromise between simplicity and accuracy has been achieved using PWS models in many works [4, 5]. However, some applications could require additional considerations to achieve equivalence between the mathematical model and real system responses, as we report in this paper.

Nonsmooth systems controlled by digital techniques can require more elaborate models depending on hardware specifications or the sensitivity of the systems. Analog-to-digital conversion (ADC) processes can modify the dynamic behavior of the system due to phenomena such as quantization level or conversion time.

Power converters are modelled as PWS due to the switching action of transistors and diodes and saturation action in the PWM controller (see, e.g., [6]). Bifurcations and chaos have been detected in many power electronic models. For a broad study of nonlinear phenomena exhibited by power converters, see [7]. On the other hand, in the last decade the ZAD strategy has been developed for controlling DC-DC buck power converters. This controller forces a defined function to have zero average for each sampling period. In this case, the function $s_{pwm}(t)$ is defined as a linear combination of the values of the error and its derivative at the switching instants (i.e., $s_{pwm}(t) := f(e(kT), \dot{e}(kT))$). Previous theoretical and numerical studies have demonstrated that the ZAD strategy offers two important advantages: very low error [8] and fixed switching frequency [9, 10]. In [10] a complete study for an ideal model of the ZAD-controlled converter was presented, when the parameter K_s varies.

In this paper, a new model for the ZAD-controlled buck power converter is introduced and the ADC process is included explicitly for acquisition of the state variables values, that is, current flowing to the inductor and voltage across the capacitor. Data acquisition by the sensors and signal digitizing by the A/D converters are two crucial processes in the performance of the ZAD controller; however, in this paper only the dynamic behavior depending on the resolution of the A/D converters is analyzed. This resolution affects the accuracy of the state variable values changing the performance of the ZAD controller. Although some authors have included digitalization effects of analog-to-digital (A/D) and digital-to-analog (D/A) converters in different systems, either linear [11, 12] or nonlinear (such as power converters) [13, 14], their main conclusions are that the ADC processes can generate limit cycles in the dynamic behavior of the systems.

The paper is organized as follows: Section 2 presents the mathematical framework to analyze and control the buck converter. Section 3 presents a detailed analysis of the quantization effects in the transition to chaos for a ZAD-controlled buck converter, introducing the model of the ADC process and changing its resolution n ($n \in \{8, 12, 16\}$). In Section 4, conclusions are presented.

2. Mathematical Model and Physical Considerations

2.1. Buck Converter

A complete study of the applications and design of power converters can be found in [15, 16]. A simplified diagram of the closed-loop synchronous buck converter is shown in Figure 1(a). Its main feature is that the output value V_o is lower than the source V_{in} (step-down converter). The switches S_1 and S_2 operate in a complementary way; that is, when S_1 is on, the switch S_2 is off and vice versa.

The mathematical model for the synchronous buck converter can be expressed in a compact form as:

$$\begin{pmatrix} \dot{x}_1 \\ \dot{x}_2 \end{pmatrix} = \begin{pmatrix} -\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} 0 \\ \frac{V_{in}}{L} \end{pmatrix} u, \quad (2.1)$$

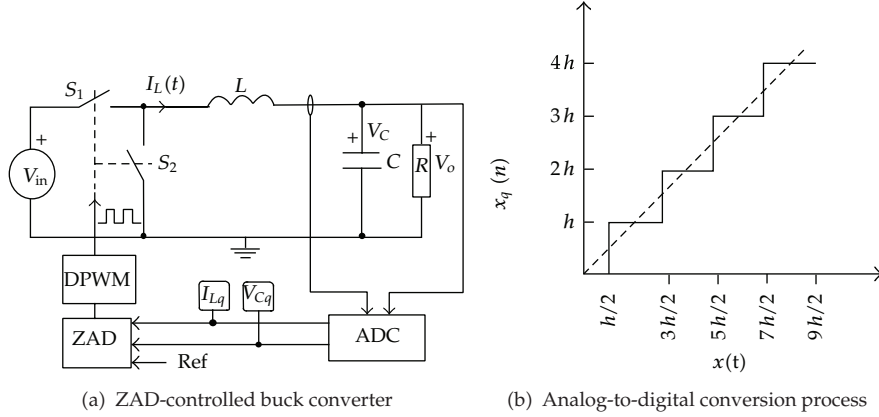


Figure 1: Schematic diagram for digitally controlled buck power converter and digital conversion process.

where $x_1 = v_C$, $x_2 = i_L$, and u belongs to discrete set $\{0, 1\}$. The objective of controlling the buck converter is related to regulation or tracking tasks. In this paper the converter is used as a regulator. The next step is to design a control strategy so that the load voltage is regulated to a desired value. the duty cycle d , which is defined as the ratio between the time that the switch S_1 is on ($u = 1$) and the sampling time T in each T ($T = 50 \mu s$ in this work). In particular the duty cycle is computed as $d = \text{sat}(D_k/T)$, and D_k is computed according to ZAD control technique as it is explained in Section 2.2. After the duty cycle is computed, the control sequence to be applied to (2.1) during one sampling time is given by

$$u = \begin{cases} 1 & \text{if } kT \leq t < kT + \frac{dT}{2}, \\ 0 & \text{if } kT + \frac{dT}{2} < t < (k+1)T - \frac{dT}{2}, \\ 1 & \text{if } (k+1)T - \frac{dT}{2} \leq t \leq (k+1)T. \end{cases} \quad (2.2)$$

2.2. ZAD Strategy

The control strategy is based on the concept of zero-average dynamics on the function s_{pwl} [9, 17, 18]. The ZAD strategy can be summarized as follows: (1) to choose dynamics that will be forced to have a zero average, (2) to force the dynamics to have zero average in each sampling period, and (3) to compute the duty cycle. As reported in [9, 19, 20], one of the possibilities for choosing the output dynamics is to define it as a piecewise-linear function given by

$$s_{pwl}(t) = \begin{cases} s_1 + (t - kT)\dot{s}_1 & \text{if } kT \leq t \leq t_1, \\ s_2 + (t - t_1)\dot{s}_2 & \text{if } t_1 < t < t_2, \\ s_3 + (t - t_2)\dot{s}_1 & \text{if } t_2 \leq t \leq (k+1)T. \end{cases} \quad (2.3)$$

Taking into account (2.2) where $u = 1$ in the first part of the interval, after $u = 0$ to finally return to $u = 1$, then each part of $s_{pwl}(t)$ is defined as

$$\begin{aligned}
 s_1 &= \left(x_1 - \text{ref} + K_s \dot{x}_1 \sqrt{(LC)} \right) \Big|_{x=x(kT), u=1}, \\
 s_2 &= \frac{D_k}{2} \dot{s}_1 + s_1, \\
 s_3 &= s_2 + (T - D_k) \dot{s}_2, \\
 \dot{s}_1 &= \dot{x}_1 + K_s \sqrt{(LC)} \dot{x}_1 \Big|_{x=x(kT), u=1}, \\
 \dot{s}_2 &= \dot{x}_1 + K_s \sqrt{(LC)} \dot{x}_1 \Big|_{x=x(kT), u=0}, \\
 t_1 &= kT + \frac{D_k}{2}, \quad t_2 = kT + T - \frac{D_k}{2}.
 \end{aligned} \tag{2.4}$$

K_s is a dimensionless positive constant and $k \in 0, 1, 2, \dots$. Therefore, the zero average condition is

$$\int_{kT}^{(k+1)T} s_{pwl}(t) dt = 0. \tag{2.5}$$

To find D_k , (2.5) is solved to obtain

$$D_k = \frac{2s_1 + T\dot{s}_2}{\dot{s}_2 - \dot{s}_1}. \tag{2.6}$$

Finally, due to saturation effects, it is necessary to limit the duty cycle based on the sampling time. The duty cycle to be applied to the system is defined as

$$d = \begin{cases} 1 & \text{if } \frac{D_k}{T} > 1, \\ \frac{D_k}{T} & \text{if } 0 \leq \frac{D_k}{T} \leq 1, \\ 0 & \text{if } \frac{D_k}{T} < 0. \end{cases} \tag{2.7}$$

2.3. Analog-to-Digital Conversion Process

As the ZAD strategy will be implemented in a digital platform, the ADC process must be included in the modelling stage. The main parts of the ADC process are sample and hold, and quantization and encoder processes [21].

2.3.1. Sample and Hold

The sample and hold process consists of catching the value of the signal to be sampled at a given instant kT (sampling) and holding it until the instant $kT + T$. Then the value of the signal $x(t) := x(kT) \forall t \in [kT, kT + T)$.

2.3.2. Quantization Process

The quantization process consists of transforming a continuous signal into a finite set of values. The quantization refers to an operation characterized by the relationship between the output signal, that is, one element of the finite discrete set, and the input signal, a continuous value. In Figure 1(b), the dashed line represents the input, and the staircase functions are the output. h is the quantization level, that is, the value of the least significant bit (LSB) of the quantization process, and it can be expressed mathematically as

$$h = \frac{V_{\text{ref}_{hi}}}{2^n}, \quad (2.8)$$

where n is the number of bits of the analog-to-digital converter and $V_{\text{ref}_{hi}} = 5 \text{ V}$ is the upper reference voltage.

3. Bifurcation Analysis

In this section, the dynamic behavior of a DC-DC buck power converter controlled by the ZAD strategy is analyzed, when the ADC process is included in the modeling stage.

The transition from periodicity to chaos in the system without the ADC process was studied in [9, 10]. Although in those papers the signal control $u \in \{-1, 1\}$, the bifurcation diagrams do not show important changes when $u \in \{0, 1\}$. The dynamic behavior of the system with 8-, 12- or 16-bit ADC resolution has significant differences from the system without an ADC process.

In this section, bifurcation diagrams of the model for different resolutions of the A/D converter are shown. Later, the observed dynamics are compared and discussion about the quantization effects is presented. In this particular case $R = 20 \Omega$, $C = 40 \mu\text{F}$, $L = 2 \text{ mH}$, and $V_{\text{in}} = 40 \text{ V}$. The desired output voltage is $\text{ref} = 32 \text{ V}$. All bifurcation diagrams are made considering the samples of the states every T seconds, that is, based on the stroboscopic map.

The system without ADC process (or with an ideal ADC process) has an asymptotically stable $1T$ -periodic orbit for values of K_s larger than 3.25. Bifurcation diagrams of a buck converter controlled with the ZAD strategy and neglecting the ADC process are presented in Figure 2. The first bifurcation occurs near $K_s = 3.25$, and it is a flip type. As K_s is reduced, the system undergoes successive smooth and nonsmooth bifurcations. Period-doubling and border-collision bifurcations generate $2T$ -, $4T$ -, and $8T$ -periodic orbits and chaotic bands with different numbers of saturated cycles, depending on nonsmooth transitions. A rigorous continuation method was applied in [19] to determinate ranges of stability and existence for the $1T$ -, $2T$ -, and $4T$ -periodic orbits. The successive smooth and nonsmooth bifurcations in a very narrow range of K_s close to 3 cause the transition from periodic orbits to chaotic bands. Band-merging processes due to crisis bifurcations are observed for $K_s \in [0.1, 3)$. The transition between one-band chaos and two-band chaos occurs near $K_s \approx 0.4$, the transition

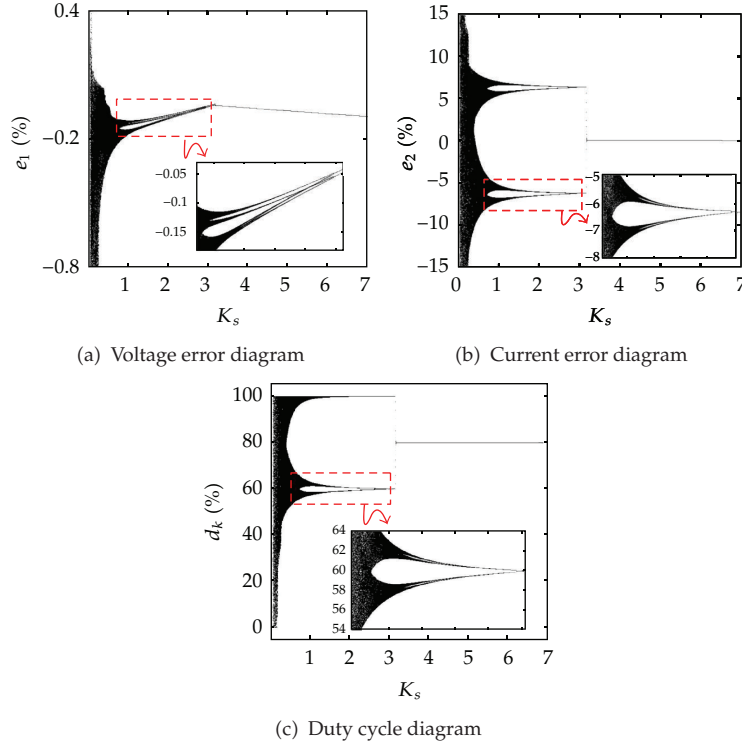


Figure 2: Bifurcation diagrams of the system without ADC process (or with an ideal ADC process).

between two-band chaos and four-band chaos is close to $K_s \approx 0.75$, and the transition between four-band chaos and eight-band chaos is close to $K_s \approx 1.2$. The period-doubling band process continues until the K_s value is close to 3.

The inclusion of the ADC process affects the dynamic behavior of the system. Technical specifications of the A/D converters, mainly their resolution, change the behavior of the ZAD-controlled buck converter. Other aspects such as resolution of the digital PWM, noise, or precision of arithmetic calculations in the digital platform also have effects on the transition to chaos. In this paper it is considered that digital PWM has infinity resolution.

Figure 3 shows bifurcation diagrams of the model with the ADC process when K_s is varied.

Three ADC resolutions are considered: 8, 12, and 16 bits. The remaining parameters are the same in all cases. To compare regulation errors, voltage error ($e_1(kT)$) and current error ($e_2(kT)$) are depicted instead of capacitor voltage ($V_C(kT)$) and inductor current ($I_L(kT)$). The variables $e_1(kT)$ and $e_2(kT)$ are defined as follows:

$$e_1(kT) = \frac{100(V_C(kT) - \text{ref})}{\text{ref}},$$

$$e_2(kT) = \frac{100(I_L(kT) - \text{ref}_2)}{\text{ref}_2}$$
(3.1)

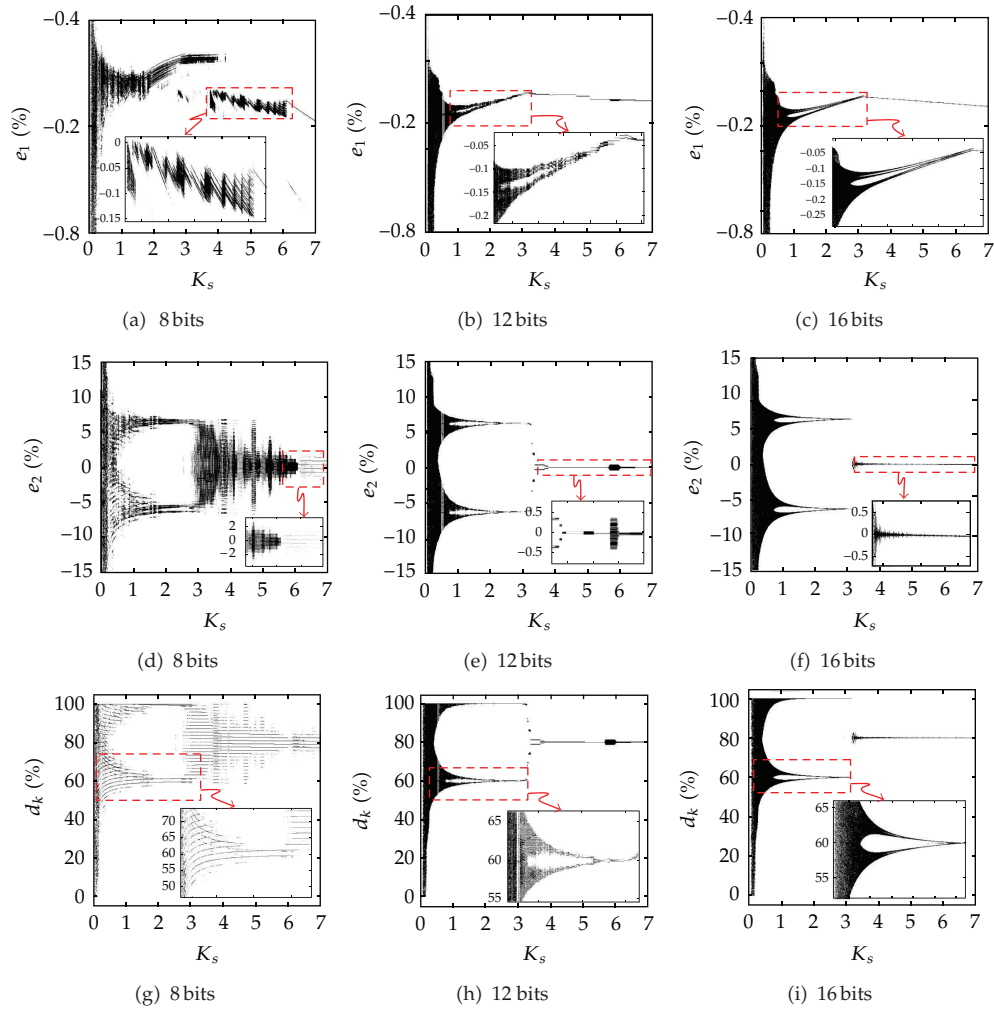


Figure 3: Bifurcation diagrams varying K_s and the ADC resolution. ((a)–(c)) Voltage error diagrams (e_1) for 8, 12 and 16 bits, respectively. ((d)–(f)) Current error diagrams (e_2) for 8, 12, and 16 bits, respectively. ((g)–(i)) Duty cycle diagrams for 8, 12, and 16 bits, respectively.

with $\text{ref}_2 = \text{ref}/R$. The quantization effects in the dynamical behavior of the system can be divided into two analyses.

- (i) Quantization effects in chaos and band chaos dynamics. In this case, the parameter K_s is bounded to the range $(0.1, 3)$, and the ADC resolution belongs to the set $\{8, 12, 16\}$.
- (ii) Quantization effects in periodic dynamics. In this case, the parameter K_s is bounded to the range $(3, 7)$, and the ADC resolution belongs to the set $\{8, 12, 16\}$.

Next, the main effects of A/D converters on aperiodic and periodic dynamics are analyzed. Interesting phenomena can be seen.

3.1. Quantization Effects in Chaos and Band Chaos Dynamics

The system without an A/D converter has a period-doubling band bifurcation scenario in the range between $K_s = 0.1$ and $K_s = 3$ (see Figure 2). The structure of the chaos and band chaos dynamics is affected by the A/D converter resolution. Drastic variations in the dynamic behavior can be observed when the A/D converter resolution is fixed to $n = 8$ bits. The band-merging process is interrupted by cascades of periodic inclusions. Only the transition between one-band chaos and two-band chaos is preserved near $K_s \approx 0.4$. Other band transitions disappear. The presence of chaos and band chaos dynamics drastically diminishes, and the sensitivity to initial conditions and coexistence of periodic solutions increase considerably. The system converges to different basins of attraction depending on the initial conditions. Dynamics with 8-bit A/D converters move to the right in the axis V_C and remain in the same range in the axis I_L . Therefore, voltage error at the sampling time ($e_1(kT)$) increases approximately from 0.2% to 0.3%, while current error ($e_2(kT)$) remains in the range between -10% and 10% (see Figures 3(a) and 3(d)).

Figures 3(b), 3(e), and 3(h) show bifurcation diagrams of the system for 12-bit ADC resolution. Overlapping cascades of periodic orbits interspersed with chaos and band chaos attractors are observed. Two band transitions are preserved: one-band chaos to two-band chaos near $K_s \approx 0.4$ and two-band chaos to four-band chaos near $K_s \approx 0.75$. The presence of chaos and band chaos increases.

An interesting phenomenon associated with the two crisis bifurcations was detected. The bifurcation diagrams (Figures 3(b), 3(e), and 3(h)) show an abrupt change of dynamic behavior between the two crisis bifurcations in the interval $K_s \in (0.54, 0.61)$. Different periodic windows can be seen depending on the initial conditions. Chaotic transients and fractal basin boundaries are also present. These phenomena have been studied in several works [22–24]. The appearance of transient chaos is relevant to the evolution of the saddle sets [25]. A chaotic saddle, also known as a nonattracting chaotic set, usually leads to chaotic transients and fractal basin boundaries [26]. In our case, the collision between the chaotic attractor and the unstable periodic orbit when the crisis occurs for $K_s \approx 0.4$ induces the formation of transient chaos and fractal basins of attraction. Figure 4 shows transient responses for $K_s = 0.55$ with different initial conditions. Small variations in V_{C0} demonstrate the extreme sensitivity to the initial conditions of the system.

However, very high periodic orbits (of order 100 or 1000) could be mistaken for chaos attractors. Some attractors have a chaotic shape, but the state variables are located with a bounded dispersion. This finding suggests the existence of a sequence with a very long periodic pattern. Figure 5 was generated to illustrate this phenomenon. State variables generated by nonsaturated duty cycles are shown in blue. State variables generated by saturated duty cycles to $d_k = 0\%$ are shown in green, and state variables generated by saturated duty cycles to $d_k = 100\%$ are shown in red.

Figures 5(a), 5(b), and 5(c) show the chaotic dynamics for the system with an ideal ADC process. A one-band chaos attractor for $K_s = 0.125$, two-band chaos attractor for $K_s = 0.5$, and four-band chaos attractor for $K_s = 1$ are presented. Any periodic pattern can be defined because the state variables are always located at different points.

The presence of chaotic dynamics diminishes as ADC resolution decreases. The system does not have chaotic attractors for any value of $K_s \in \{0.125, 0.5, 1\}$ if the AD converter has 8-bit resolution. Different periodic orbits are observed: an $8T$ -periodic orbit with seven nonsaturated cycles and one saturated cycle to $d_k = 100\%$ for $K_s = 0.5$ (Figure 5(k)) and an $18T$ -periodic orbit with 14 nonsaturated cycles and 4 saturated cycles to $d_k = 100\%$ for

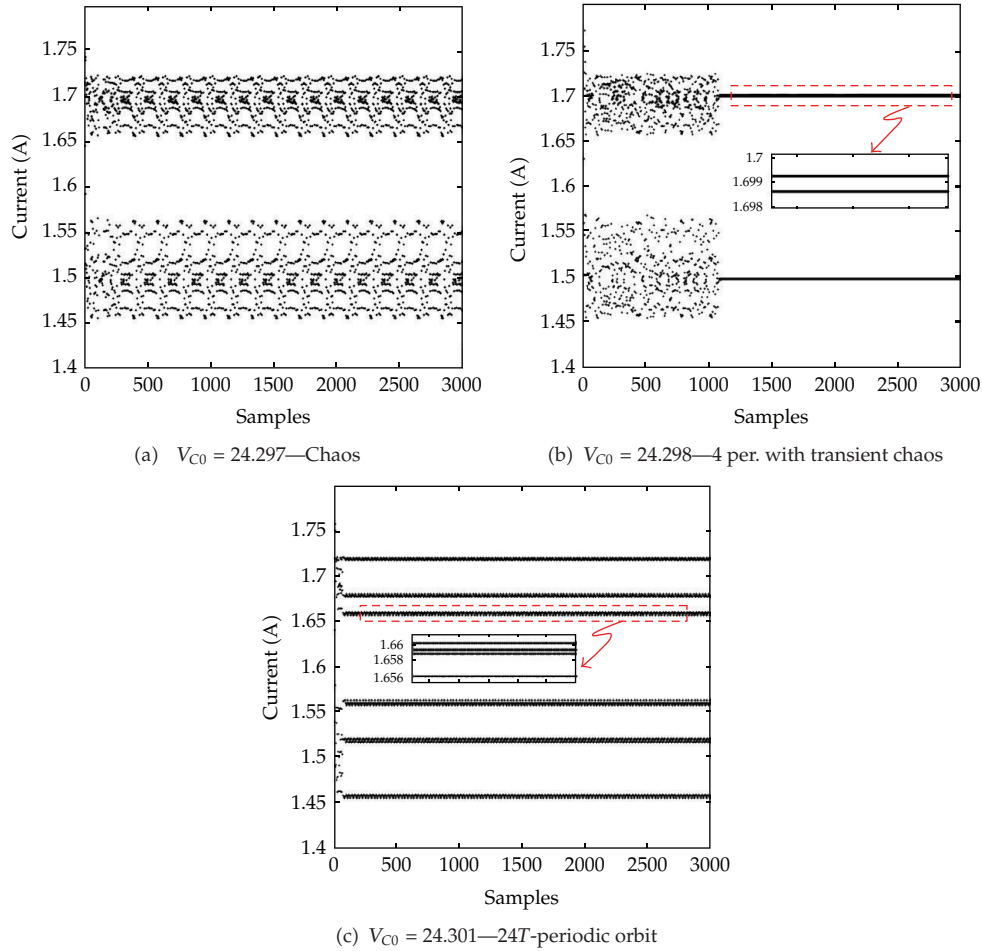


Figure 4: Transient responses of the system for 12-bit ADC resolution and different voltage initial conditions V_{C0} . The ZAD parameter is $K_s = 0.55$ and the current initial condition (I_{L0}) is 1.8.

$K_s = 1$ (Figure 5(l)). The attractor for $K_s = 0.125$ has a chaotic shape, but the state variables are located in a finite set of values. The size of this set is near 200; therefore, the periodicity of this attractor is near 200 (Figure 5(j)).

The same situation occurs with the attractors generated with 12-bit ADC resolution. Attractors generated with K_s in the set $\{0.125, 0.5, 1\}$ have chaotic shapes, but the state variables are located in sets of finite size. The size of these sets is of the order of 1000. See Figures 5(g), 5(h), and 5(i).

Figures 3(c), 3(f), and 3(i) show the bifurcation diagrams of the system for 16-bit ADC resolution. These bifurcation diagrams are very close to the responses for an ideal ADC process. The band-merging process is observed without significant changes. Three band transitions are distinguished: one-band to two-band near $K_s \approx 0.4$, two-band to four-band transition near $K_s \approx 0.75$, and four-band to eight-band transition near $K_s \approx 1.2$. The presence of chaos and band chaos dynamics is more clear. Attractors generated with K_s in the set $\{0.125, 0.5, 1\}$ have chaotic shapes and the dispersion of state variables is very close to the ideal case. All numerical proofs indicate that the responses shown in Figures 5(d), 5(e), and

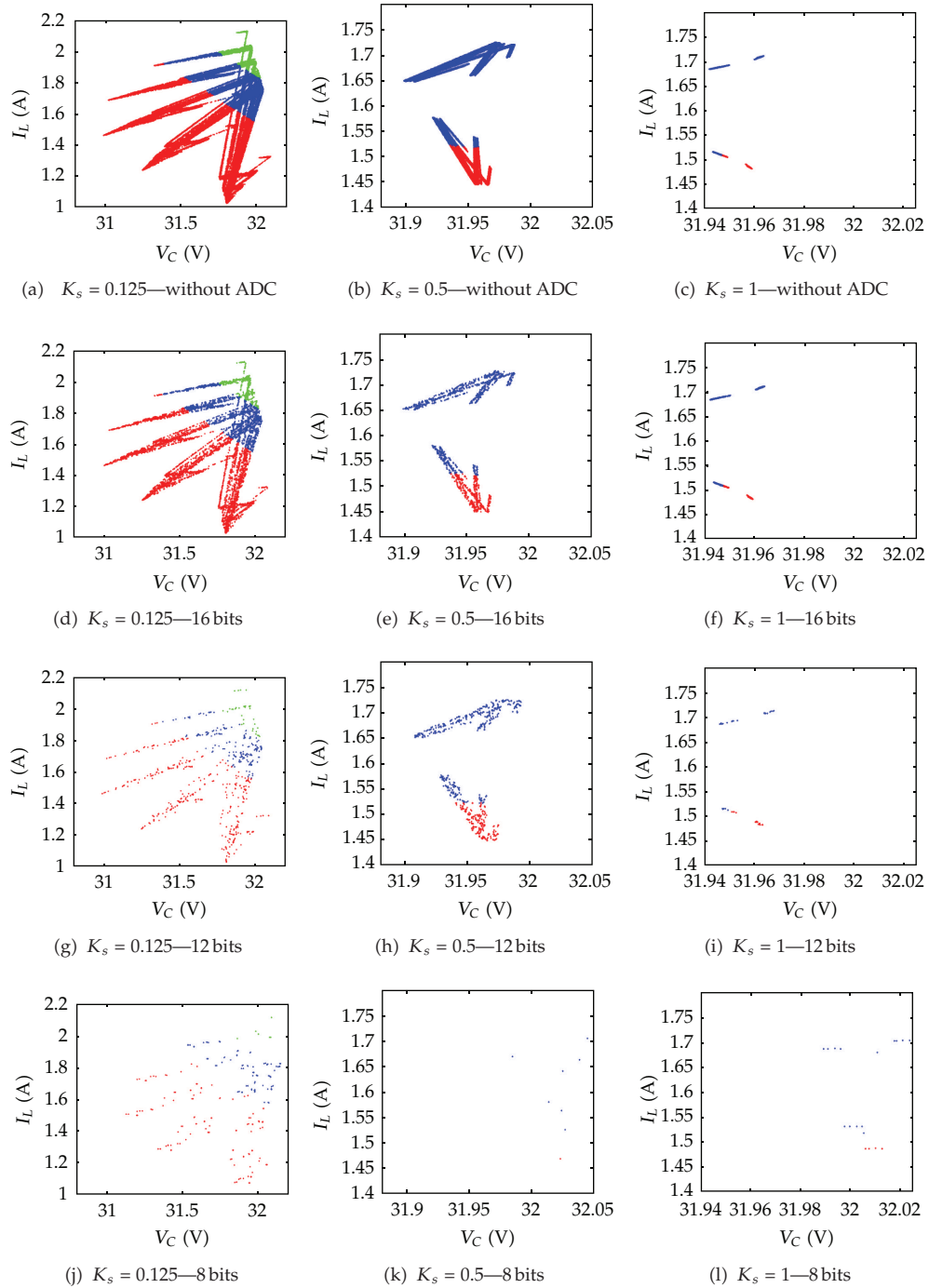


Figure 5: V_C versus I_L phase portraits varying K_s and the ADC resolution. ((a), (d), (g), (j)) $K_s = 0.125$ without and with 16-, 12-, and 8-bit ADC, respectively. ((b), (e), (h), (k)) $K_s = 0.5$ without and with 16-, 12-, and 8-bit ADC, respectively. ((c), (f), (i), (l)) $K_s = 1$ without and with 16-, 12-, and 8-bit ADC, respectively.

Table 1: Variation of the mean values and standard deviations of the state variables when the ADC resolution is varied and $K_s = 0.125$.

n	mn (V_C) [V]	mn (I_L) [A]	std (V_C) [V]	std (I_L) [A]
2	34.2861	1.7138	4.0534	1.0586
4	32.3086	1.6155	0.2946	0.2923
6	31.8776	1.5940	0.5102	0.2898
8	31.7666	1.5886	0.2693	0.2427
10	31.7014	1.5853	0.2494	0.2516
12	31.6907	1.5847	0.2471	0.2488
14	31.6884	1.5846	0.2466	0.2493
16	31.7022	1.5854	0.2459	0.2431

Table 2: Variation of the mean values and standard deviations of the state variables when the ADC resolution is varied and $K_s = 1$.

n	mn (V_C) [V]	mn (I_L) [A]	std (V_C) [V]	std (I_L) [A]
2	35.5555	1.7778	0.4310	0.2999
4	32.3764	1.6191	0.2086	0.2097
6	32.1625	1.6086	0.0115	0.0999
8	32.0059	1.6008	0.0099	0.0932
10	31.9680	1.5989	0.0058	0.0999
12	31.9575	1.5983	0.0076	0.1000
14	31.9537	1.5981	0.0074	0.1002
16	31.9529	1.5981	0.0074	0.1002

5(f) are chaos and band chaos dynamics. In these cases, the possibility of extremely high periodic patterns is not considered because the dispersion of the state variables cannot be limited to a finite set.

Although the dynamic properties show important variations when ADC resolution is varied, the statistical properties are not significantly modified. Table 1 shows the evolution of the mean value and standard deviations when the ADC resolution is varied between 2 bits and 16 bits for $K_s = 0.125$. Differences between chaotic dynamics and very high periodic orbits are not detected by these statistical measures. However, the results of this table confirm that 8- or fewer-bit A/D converter resolution affects the regulation condition of the system. Table 2 summarizes the same test for $K_s = 1$, when the ideal model has four-band chaos. These results are very close when the ADC resolution is 10, 12, 14, or 16.

3.2. Quantization Effects in Periodic Dynamics

The system without an A/D converter has a $1T$ -periodic orbit for $K_s \in (K_c, 7)$. At $K_s = K_c \approx 3.25$, the system experiences a flip bifurcation, and a stable $2T$ -periodic orbit exists for $K_s \in (3, K_c)$. Significant changes in the dynamical behavior can be observed for 8-bit ADC resolution; periodic and quasiperiodic orbits are induced in the range $K_s \in (3, 7)$.

Quasiperiodic and periodic dynamics coexist when the resolution of the ADC converter is fixed to 8 bits and the range of $K_s \in (3, 6)$, while coexisting periodic solutions

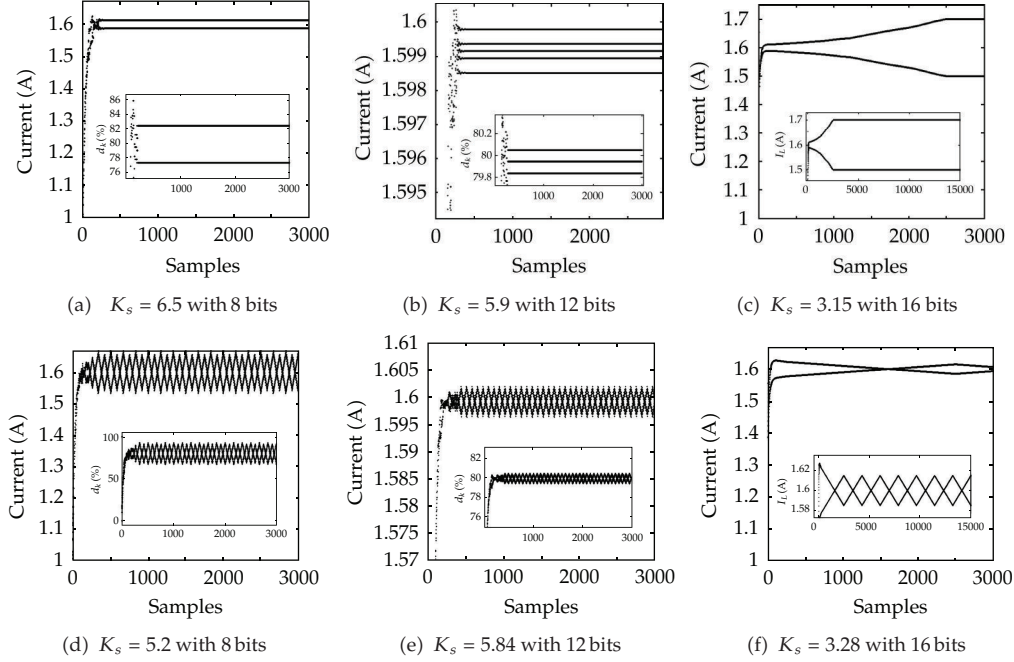


Figure 6: Examples of periodic and quasi periodic orbits for the system with 8-, 12-, and 16-bit ADC, respectively.

are detected when $K_s > 6$. Figure 6(d) shows an example of a quasiperiodic dynamic of the system for an 8-bit ADC process and $K_s = 5.2$. Low-frequency oscillation is induced by the ADC process. Figure 6(a) shows an example of a $2T$ -periodic orbit when $K_s = 6.5$. Other periodic dynamics are also possible depending on the initial conditions. Coexistence phenomena will be analyzed shortly.

Periodic and quasiperiodic orbits can be identified for 12-bit ADC resolution depending on K_s and the initial conditions. Periodic behavior can be interrupted by quasiperiodic windows and extreme sensitivity to initial conditions can be distinguished. Figures 6(b) and 6(e) show examples of periodic and quasiperiodic orbits in the system with a 12-bit ADC process.

Dynamic behavior for 16-bit ADC resolution is very close to the behavior with an ideal ADC process. Quasiperiodic behavior can be detected near the flip transition for $K_s \approx 3.25$. The induced oscillation has lower frequency than the cases with 8 and 12 bits. See Figure 6(f).

Statistical measures show that the dynamic behavior tends toward the response of the ideal ADC process when ADC resolution is increased. Table 3 summarizes the mean values and standard deviations of state variables when ADC resolution is varied from $n = 2$ to $n = 16$ and $K_s = 4.5$.

Coexistence of dynamics is the most interesting and representative phenomenon detected in these bifurcation scenarios. A particular case when the ZAD parameter is fixed to $K_s = 6.5$ and ADC resolution is selected from the set $\{8, 12, 16\}$ is presented in the following.

Three common characteristics were identified in the three cases:

- (i) multiple coexisting periodic solutions depending on the initial conditions,
- (ii) fractal basin boundaries characterized by extreme sensitivity to the initial values,

Table 3: Variation of the mean values and standard deviations of the state variables when the ADC resolution is varied and $K_s = 4.5$.

n	mn(V_C) [V]	mn(I_L) [A]	std(V_C) [V]	std(I_L) [A]
2	28.5714	1.4286	0.1832	0.2888
4	31.5433	1.5776	0.0010	0.1060
6	32.1952	1.6103	0.0067	0.0389
8	31.9844	1.5997	0.0022	0.0073
10	31.9896	1.6000	0.0006	0.0036
12	31.9814	1.5996	0.0001	0.0005
14	31.9806	1.5995	0.0001	0.0004
16	31.9804	1.5995	0.0000	0.0006

Table 4: Examples of coexisting periodic orbits for 8-bit ADC resolution and $K_s = 6.5$. $I_{L0} = 1.5$.

Case	(V_{C0}, I_{L0}) ([V], [A])	Orb.	Duty cycle characteristics
1	(0.4, 1)	1 per.	$d_1 = 79.53\%$
2	(0, 1)	2 per.	$d_1 = 79.09\%$ and $d_2 = 80.78\%$
3	(0.1, 1)	2 per.	$d_1 = 77.4\%$ and $d_2 = 82.47\%$
4	(0.5, 1)	2 per.	$d_1 = 77.85\%$ and $d_2 = 81.22\%$
5	(4.9, 1)	2 per.	$d_1 = 75.71\%$ and $d_2 = 84.16\%$
6	(32.4, 2)	2 per.	$d_1 = 72.34\%$ and $d_2 = 87.53\%$
7	(20.2, 0)	2 per.	$d_1 = 74.47\%$ and $d_2 = 84.6\%$
8	(14.3, 0)	2 per.	$d_1 = 76.16\%$ and $d_2 = 82.91\%$
9	(32.9, 2)	3 per.	$d_{1,2} = 79.89\%$ and $d_2 = 81.58\%$
10	(33.6, 2)	6 per.	$d_{1,3} = 74.83\%$, $d_5 = 76.51\%$, $d_{4,6} = 84.96\%$ and $d_2 = 86.65\%$
11	(33.6, 1)	6 per.	$d_{1,3} = 73.14\%$, $d_5 = 74.83\%$, $d_{4,6} = 86.65\%$ and $d_2 = 88.33\%$
12	(33.9, 1)	6 per.	$d_{1,3} = 76.51\%$, $d_5 = 78.2\%$, $d_{4,6} = 83.27\%$ and $d_2 = 84.96\%$
13	(32.6, 2)	10 per.	$d_{1,3,5} = 78.65\%$, $d_{6,7,8,9,10} = 80.34\%$ and $d_{2,4} = 82.02\%$
14	(32.5, 2)	10 per.	$d_{1,3,5} = 76.96\%$, $d_{7,9} = 78.65\%$, $d_{6,8,10} = 82.02\%$ and $d_{2,4} = 83.71\%$
15	(32.54, 1.247)	11 per.	$d_{1,3,5} = 78.65\%$, $d_{6,7,8,9,10,11} = 80.34\%$, $d_{6,8,10} = 82.02\%$ and $d_{2,4} = 82.02\%$
16	(32.24, 1.357)	22 per.	$d_{1,3,5} = 76.96\%$, $d_{7,9,11,17,19,21} = 78.65\%$, $d_{12,13,14,15,16} = 80.34\%$, $d_{6,8,10,18,20,22} = 82.02\%$, and $d_{2,4} = 83.71\%$

(iii) duty cycle sequences of coexisting periodic solutions are composed by nonsaturated values; that is, $0\% < d < 100\%$. Additionally, some nonsaturated duty cycles can be the same for two or more coexisting solutions. Small changes in a duty cycle value or in a recurrence pattern produce different periodic solutions.

Table 4 summarizes the characteristics of sixteen periodic orbits for $K_s = 6.5$ and 8-bit ADC resolution. Also, $1T$ -, $2T$ -, $3T$ -, $6T$ -, $10T$ -, $11T$ -, and $22T$ -periodic orbits are possible depending on the initial conditions of the voltage capacitor V_{C0} and inductor current I_{L0} . Figure 7 shows the evolution of several cases presented in Table 4. For $V_{C0} = 0.4$ and $I_{L0} = 1$ there is a stable $1T$ -periodic orbit. The $1T$ -periodic orbit is characterized by a duty cycle of 79.53%, reaching low stationary error and fixed-frequency condition.

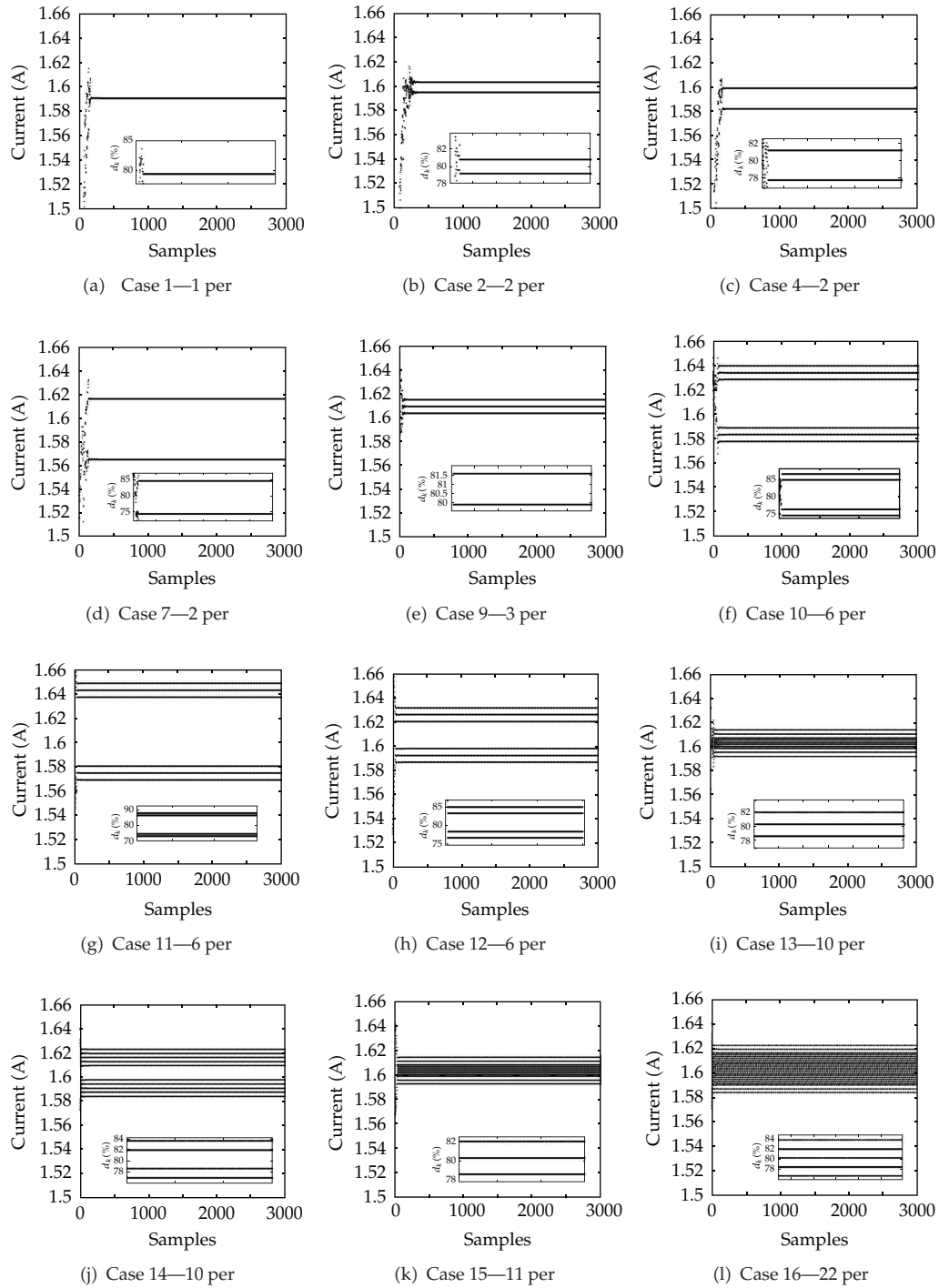


Figure 7: Examples of coexisting periodic orbits for 8-bit ADC resolution and $K_s = 6.5$. More analysis is presented in Table 4.

Table 5: Examples of coexisting periodic orbits for 12-bit ADC resolution and $K_s = 6.5$. $I_{L0} = 1.5$.

Case	V_{C0} [V]	Orb.	Duty cycle characteristics
1	30.04	3 per.	$d_{1,2} = 79.92\%$ and $d_3 = 80.02\%$
2	30.22	6 per.	$d_{1,3} = 79.81\%$, $d_5 = 79.92\%$, $d_{4,6} = 80.02\%$ and $d_2 = 80.13\%$
3	33.79	6 per.	$d_1 = 79.76\%$, $d_{3,5} = 79.86\%$, $d_4 = 80.07\%$ and $d_{2,6} = 80.18\%$
4	33.34	6 per.	$d_1 = 79.86\%$, $d_{3,4,5} = 79.97\%$ and $d_{2,6} = 80.07\%$
5	32.14	11 per.	$d_1 = 79.68\%$, $d_{3,10} = 79.79\%$, $d_{5,8} = 79.89\%$ $d_{6,7} = 80\%$, $d_{4,9} = 80.1\%$ and $d_{2,11} = 80.21\%$
6	32	18 per.	$d_1 = 79.57\%$, $d_{3,17} = 79.68\%$, $d_{5,15} = 79.79\%$, $d_{7,10,13} = 79.89\%$ $d_{8,9,11,12} = 80\%$, $d_{6,14} = 80.1\%$, $d_{4,16} = 80.21\%$ and $d_{2,18} = 80.31\%$
7	30.63	22 per.	$d_{1,3,7,9} = 79.81\%$, $d_{5,11,12,14,15,17,18,20,21} = 79.92\%$ $d_{4,6,10,13,16,19,22} = 80.02\%$ and $d_{2,8} = 80.13\%$
8	31.99	22 per.	$d_1 = 79.57\%$, $d_{3,21} = 79.68\%$, $d_{5,12,19} = 79.79\%$, $d_{7,10,14,17} = 79.89\%$ $d_{8,9,15,16} = 80\%$, $d_{6,11,13,18} = 80.1\%$, $d_{4,20} = 80.21\%$ and $d_{2,22} = 80.31\%$
9	32.02	22 per.	$d_1 = 79.47\%$, $d_{3,21} = 79.57\%$, $d_{5,19} = 79.68\%$, $d_{7,17} = 79.79\%$, $d_{9,12,15} = 79.89\%$, $d_{10,11,13,14} = 80\%$, $d_{8,16} = 80.1\%$, $d_{6,18} = 80.21\%$, $d_{4,20} = 80.31\%$ and $d_{2,22} = 80.42\%$
10	30.02	34 per.	$d_{1,3,7,9,13,15} = 79.81\%$, $d_{5,11,17,18,20,21,23,24,26,27,29,30,32,33} = 79.92\%$ $d_{4,6,10,12,16,19,22,25,28,31,34} = 80.02\%$, $d_{2,8,14} = 80.13\%$

Seven possibilities for $2T$ -periodic orbits are detected. All of them are defined by two nonsaturated cycles (d_1 and d_2). The $3T$ -periodic dynamics can be obtained with a duty cycle sequence (d_1, d_2, d_3) where $d_1 = d_2 = 79.89\%$ and $d_3 = 81.58\%$. Figure 7(g) shows the evolution of the $3T$ -periodic orbit.

The $6T$ -periodic orbits are defined by duty cycle sequences ($d_1, d_2, d_3, d_4, d_5, d_6$) with four different values, where $d_1 = d_3$ and $d_4 = d_6$. Two possibilities for $10T$ -periodic orbits are identified depending on the duty cycle sequence. Both options have four different values. The first has $d_1 = d_3 = d_5$, $d_2 = d_4$, and $d_6 = d_7 = d_8 = d_9 = d_{10}$, and the second has $d_1 = d_3 = d_5$, $d_2 = d_4$, $d_7 = d_9$, and $d_6 = d_8 = d_{10}$. The $11T$ - and $22T$ -periodic orbits are possible with four and five different values of the duty cycle, respectively.

The presence of multiple coexisting periodic orbits diminishes as ADC resolution increases. Ten different stable periodic orbits were detected in the fractal basin boundaries for 12-bit ADC, but only six coexisting periodic orbits were detected for the 16-bit ADC case. Additionally, the range of variation of the state variables becomes narrower as ADC resolution increases. The current is confined to the range (1.56, 1.66) for 8-bit ADC, to (1.596, 1.602) for 12-bit ADC, and to (1.5985, 1.5995) for 16-bit ADC.

Table 5 and Figure 8 summarize the dynamics found for 12-bit ADC resolution, while Table 6 and Figure 9 summarize the case for 16-bit ADC.

4. Conclusions

In this paper, the dynamic behavior of a DC-DC buck power converter controlled by the ZAD strategy when the ADC process is included in the modeling stage is analyzed. It has been shown that the dynamic behavior of the system with an ADC process has very important changes compared to the ideal system (without ADC). However, if $K_s > 3.5$ and depending

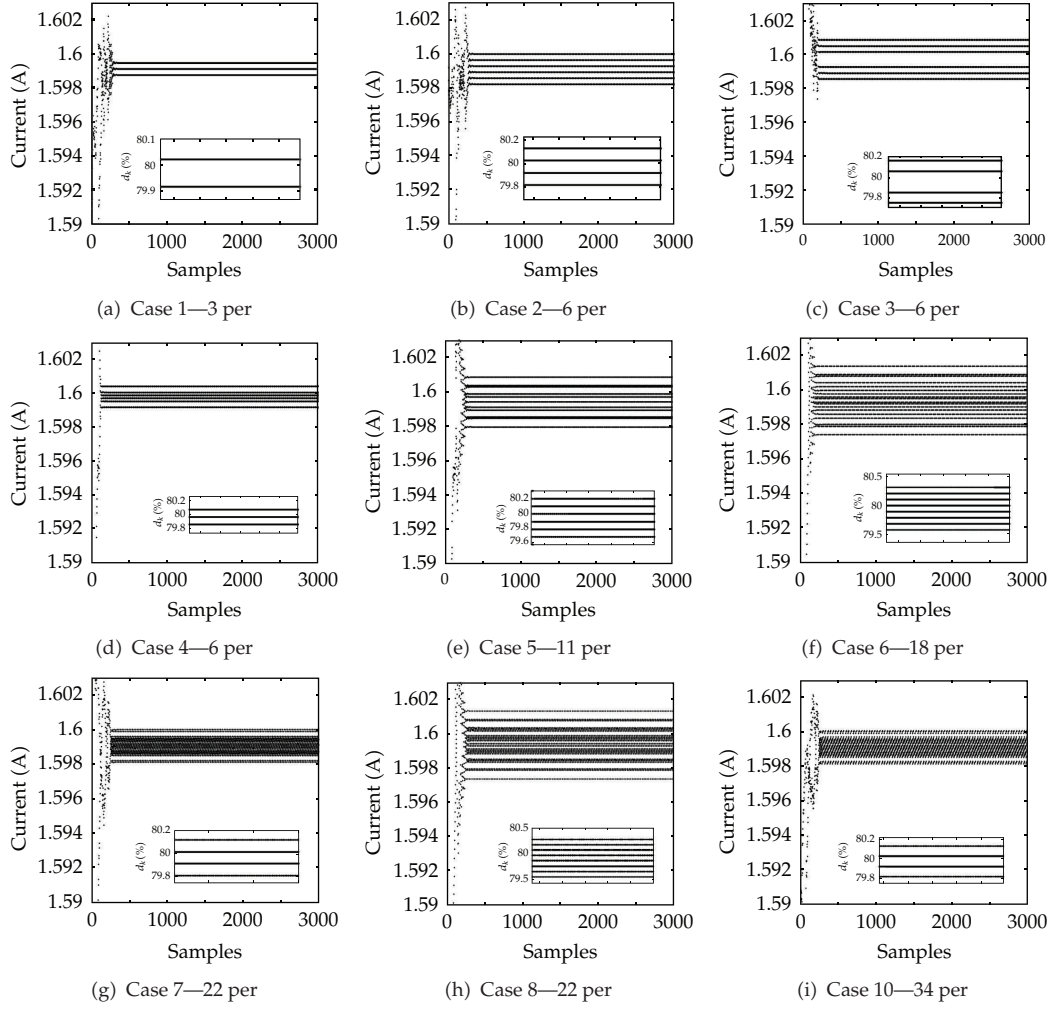


Figure 8: Examples of coexisting periodic orbits for 12-bit ADC resolution and $K_s = 6.5$. More analysis is presented in Table 5.

Table 6: Examples of coexisting periodic orbits for 16-bit ADC resolution and $K_s = 6.5$. $I_{L0} = 1.5$.

Case	V_{C0} [V]	Orb.	Duty cycle characteristics
1	32.3905	1 per.	$d_1 = 79.956\%$
2	32.055	2 per.	$d_1 = 79.877\%$ and $d_2 = 80.035\%$
3	30.22	7 per.	$d_1 = 79.946\%$, $d_{3,4,5,6} = 79.953\%$ and $d_{2,7} = 79.959\%$
4	30.01	14 per.	$d_1 = 79.926\%$, $d_{3,5,11,13} = 79.933\%$, $d_{7,9} = 79.94\%$ $d_8 = 79.966\%$, $d_{4,6,10,12} = 79.973\%$ and $d_{2,14} = 79.979\%$
5	30.05	14 per.	$d_1 = 79.933\%$, $d_{3,5,11,13} = 79.94\%$, $d_{7,9} = 79.946\%$ $d_8 = 79.959\%$, $d_{4,6,10,12} = 79.966\%$ and $d_{2,14} = 79.973\%$
6	30.09	26 per.	$d_{1,3,5,7,9,11,13} = 79.949\%$, $d_{14,15,16,17,18,19} = 79.956\%$ and $d_{2,4,6,8,10,12} = 79.962\%$

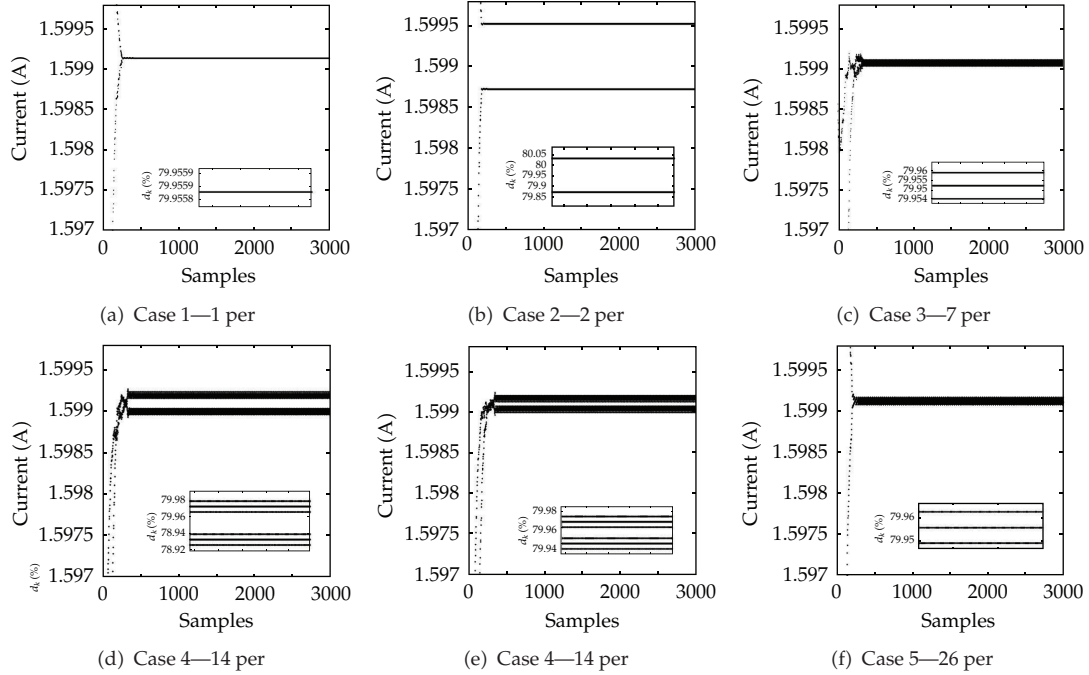


Figure 9: Examples of coexisting periodic orbits for 16-bit ADC resolution and $K_s = 6.5$. More analysis is presented in Table 6.

on the application, 8-, 12- or 16-bit ADC resolutions are enough to reach $1T$ periodic orbit with low regulation error.

It has been determined that the ADC process has global consequences in the dynamical behavior of the system. Global phenomena such as the coexistence of periodic and aperiodic attractors, fractal basin boundaries, or transient chaos are exclusively caused by the A/D converters.

A route to chaos of the ZAD-controlled buck converter without an ADC process has been studied in many works [9, 10, 19]. In all works, this bifurcation scenario has been studied using local techniques based on the Jacobian matrix, the Lyapunov exponents, and the Floquet exponents. Smooth and nonsmooth bifurcations do not have a global incidence and the dynamics do not depend on initial conditions. Few results of the global dynamics can be obtained analytically due to the difficulty involved. Therefore, the numerical analysis for the global dynamics is usually the main approach [25].

We have numerically studied the quantization effects on chaos and periodic dynamics when the resolution of the A/D converters is varied in the set $\{8, 12, 16\}$. We have shown that these effects cannot be detected using statistical measures.

It has been detected that the doubling band transitions depend on ADC resolution. Only the transition from one-band chaos to two-band chaos is preserved for 8 bits, two-band transitions are preserved for 12 bits, and three-band transitions are preserved for 16 bits.

Band-merging process interrupted by cascades of periodic inclusions was detected.

Paradoxical behavior can be distinguished. The ADC process diminishes the presence of chaos dynamics, but the sensitivity to initial conditions strongly increases. Therefore, the long-term behaviors can be classified as high or very high periodic orbits, but fractal basin

boundaries result in several possible long-term behaviors that depend heavily on initial value.

Period doubling route to chaos with an ideal ADC process is perturbed by quasiperiodic dynamics when ADC is included in the model. Other authors have studied the effects of ADC process in the dynamic behavior of the systems [11–14] and quasiperiodic route to chaos [27, 28], but as far as we know, the inclusion of quasiperiodic dynamics in route to chaos due to a quantization process has not been reported in the literature.

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