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Research Article

Models for Master-Slave Clock Distribution Networks with Third-Order Phase-Locked Loops

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The purpose of this work is to study the processing and transmission of clock signals in networks of geographically distributed nodes, in order to derive conditions for frequency and phase synchronization between the nodes. The focus is on the master-slave architecture, which presents a priority scheme of clock distribution. One-way master-slave (OWMS) and two-way master-slave (TWMS) chains are studied, considering that the slave nodes are third-order phase-locked loops (PLLs). Third-order PLLs are chosen to improve the transient response but, if their parameters are not well adjusted, stability problems and chaotic behaviors appear, restricting the lock-in range of the network. Lock-in range for third-order PLLs with Sallen-Key filter is determined and it is verified whether this range is reduced when the PLLs are connected to a network. Numerical experiments show how chain size changes the lock-in ranges and the acquisition times.

1. Introduction

The distribution of clock signals is essential for several applications in control and communication [1] establishment of a worldwide time schedule system, synchronization of oscillators at different multiplexing points in digital telecommunication networks, control and monitoring of performance at specific instants in industrial processes and establishment of a synchronous state in a supercomputer composed of several processors.

In this work, the distribution of clock signals in telecommunications networks is considered. The problem concerns mainly to the distribution of phase and frequency signals

through nodes distributed in a certain geographic area. There are three different implementation strategies: plesiochronous, master-slave (MS), and synchronous full-connected [2].

Plesiochronous networks are used when the synchronism is not critical. Oscillators with small frequency deviation are used in each node. They are manually adjusted and control signals are not needed. These networks are easy to implement, robust, though costly.

In synchronous full-connected networks, all the nodes have their own oscillator interchanging reference signals. They are more complex to be implemented, being used only in special applications, as in military communication networks.

Master-slave networks present a priority scheme of clock distribution, establishing a hierarchy between the nodes. There is a node with an extremely precise atomic oscillator, called master. The other nodes are controlled by the master's reference signal and are called slaves. As the control is centralized, if the master fails, the performance of the whole network is spoiled. However, due to its simple implementation and low cost, the master-slave networks are widely used in robotics and public telecommunications networks.

There are two types of MS networks, OWMS and TWMS. In the OWMS architecture, mainly used in telecommunication networks, the clock signal generated by the master is transmitted to the nodes sequentially, not considering the state of the slaves. In the TWMS, mainly used in process-control networks, the reference signal considers the master and the state of the slaves.

Here, the two distribution schemes are considered and compared from the lock-in point of view, with the slaves being third-order PLLs [3]. First, the isolated third-order PLL is considered and modeled, with an analytical determination of its lock-in range. Then, chains with third-order PLLs as slaves are explored by using numerical experiments.

2. Third-order PLL

The phase-locked loop (PLL) is an electronic device that has been used since 1932 in applications that demand automatic control of frequency. It is composed of a phase-detector (PD), a lowpass filter (F) and a voltage controlled oscillator (VCO) [4], as shown in Figure 2.1, and is used to extract the time basis in a reliable way, synchronizing the input signal $v_i(t)$ with the one of its internal oscillator (VCO) $v_o(t)$.

The nonlinear behavior of the PLL is due the phase detector (PD), which is represented by a signal multiplier that compares the phases of the input signal, $v_i(t)$, and the VCO output, $v_o(t)$. This operation is described by

$$v_d(t) = k_d v_i(t) v_o(t), \tag{2.1}$$

where k_d is the PD gain, and $v_i(t)$ and $v_o(t)$ have periodic expressions with central angular frequency $\omega_M(t)$ and instantaneous phases $\theta_i(t)$ and $\theta_o(t)$, respectively, as described

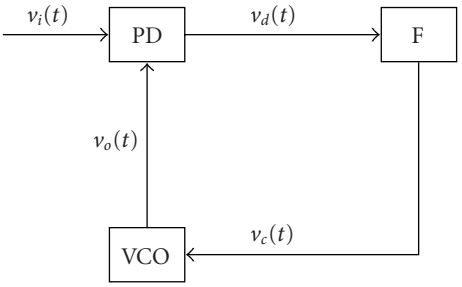


Figure 2.1. PLL block diagram.

below:

$$\begin{aligned} v_i(t) &= V_i \sin\left[\omega_M t + \theta_i(t)\right], \\ v_o(t) &= V_o \sin\left[\omega_M t + \theta_o(t)\right]. \end{aligned} \tag{2.2}$$

Combining (2.1), (2.2), $v_d(t)$ can be expressed as

$$v_d(t) = \frac{k_m V_i V_o}{2} \sin\left[2\omega_M t + \theta_i(t) + \theta_o(t)\right] + \frac{k_m V_i V_o}{2} \sin\left[\theta_i(t) - \theta_o(t)\right], \tag{2.3}$$

where k_m is the multiplier gain, being $k_d = k_m V_o/2$.

In expression (2.3), the presence of a second-harmonic term can be noticed. The signal $v_d(t)$ passes through the lowpass filter (F) to eliminate this high-frequency term called double-frequency jitter [5]; however, a small amplitude double-frequency term remains. This jitter is responsible for oscillations around the synchronous state, causing disturbances in the network performance [6].

The VCO signal is controlled by the filter output and its frequency is given by

$$\dot{\theta}_o(t) = k_o v_c(t), \tag{2.4}$$

where k_o is the VCO gain.

The VCO output has a phase $\theta_o(t)$. When the phase error $\varphi(t) = \theta_i(t) - \theta_o(t)$ has a constant value or, equivalently, the frequency error $\dot{\varphi}(t) = \dot{\theta}_i(t) - \dot{\theta}_o(t)$ is zero, the system is in the synchronous state.

First-order filters, implying second-order PLLs, are normally chosen due to their inherent stability and good lock-in range [7]. However, these PLLs frequently present high-level double-frequency terms in the PD output, as a phase-jitter, as it is difficult to adapt a first-order filter that eliminates these components in a satisfactory way. In order to eliminate this double-frequency jitter and to improve the transitory responses, higher-order filters are chosen, implying PLLs with order greater than 2.

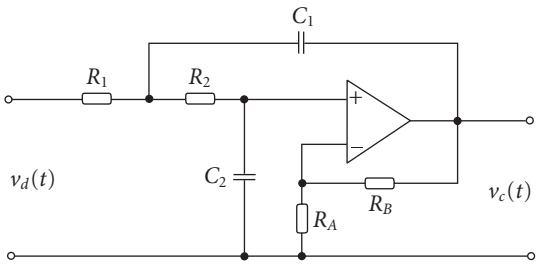


Figure 2.2. Sallen-Key second-order filter.

Here, a second-order Sallen-Key filter as shown in Figure 2.2, is chosen [7], resulting in a third-order PLL. The filter transfer function is given by

$$H(s) = \frac{V_c(s)}{V_d(s)} = \frac{K\omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}, \tag{2.5}$$

where $\omega_0^2 = 1/R_1R_2C_1C_2$, $K = 1 + R_B/R_A$ and $Q = 1/\omega_0[C_2(R_1 + R_2) + R_1C_1(1 - K)]$.

Considering the normalization of the cut-off frequency, that is, $R_1 = R_2 = C_1 = C_2 = 1$, and the PLL gain as $G = k_d k_0 V_i V_o/2$, combining (2.3), (2.4) and (2.5), and neglecting the high-frequency terms of (2.4), the dynamic equation of the third-order PLL becomes

$$\dddot{\varphi} + (3 - K)\ddot{\varphi} + \dot{\varphi} + KG\sin\varphi = \dddot{\theta}_i + (3 - K)\ddot{\theta}_i + \dot{\theta}_i. \tag{2.6}$$

Considering phase-ramp inputs, $\theta_i = \Omega t + \psi$, the dynamic equation becomes

$$\dddot{\varphi} + (3 - K)\ddot{\varphi} + \dot{\varphi} + KG\sin\varphi = \Omega. \tag{2.7}$$

Equation (2.7) describes the third-order PLL, considering $\varphi \in (-\pi, \pi]$ and $\Omega > 0$. The synchronous state corresponds to a constant phase error φ, and to frequency and acceleration errors, $\dot{\varphi}$ and $\ddot{\varphi}$, equal to zero.

3. Lock-in range

The set of parameters and inputs corresponding to a reachable asymptotically stable synchronous state for (2.7) is called lock-in range. Consequently, the lock-in range is the set of filter gains K, input frequencies Ω, and PLL gains G corresponding to the existence of an asymptotically stable synchronous state $(\varphi, \dot{\varphi}, \ddot{\varphi}) = (\varphi^*, 0, 0)$ for (2.7).

Analyzing (2.7), the synchronous state is $(\varphi, \dot{\varphi}, \ddot{\varphi}) = (\arcsin(\Omega/KG), 0, 0)$, implying a first existence condition $\Omega \leq KG$.

For $\Omega = KG$, there is the synchronous state $(\pi/2, 0, 0)$ that is nonhyperbolic [8]. For $\Omega < KG$, there are two synchronous states: $(\varphi_1, 0, 0)$ and $(\varphi_2, 0, 0)$, so that $\sin\varphi_1 = \sin\varphi_2 = \Omega/KG$, and $\cos\varphi_1 = -\cos\varphi_2 = \sqrt{1 - (\Omega/KG)^2}$. The first state can be stable depending on the parameters combination. The second one is unstable.

The stability of the synchronous states, $(\varphi_1, 0, 0)$ and $(\varphi_2, 0, 0)$ can be analyzed by using the characteristic polynomial related to the linear approximation of (2.7), around the

equilibrium states

$$P(\lambda) = \lambda^3 + (3-K)\lambda^2 + \lambda + KG\cos\varphi_{SS}. \tag{3.1}$$

The stability of the synchronous state (SS) is given by the real-part of the roots of $P(\lambda)$. If they are all negative, the corresponding synchronous state is asymptotically stable. If there is a root with positive real part, the corresponding synchronous state is unstable.

According to the Routh-Hurwitz stability criterion [9], the number of positive real-part roots of the polynomial is equal to the number of signal changes in coefficients of the first column of Routh-Hurwitz matrix R_0. For $P(\lambda)$ given by (3.1), R_0 is as follows:

$$R_0 = \begin{bmatrix} 1 & 1 \\ 3-K & KG\cos\varphi \\ \dfrac{3-K-KG\cos\varphi}{3-K} & 0 \\ KG\cos\varphi & 0 \end{bmatrix}. \tag{3.2}$$

As the synchronous state $(\varphi_2, 0, 0)$ has a negative cosine, observing R_0 and according to the Routh-Hurwitz criterion, it can be seen that the first term of the first column is positive and the fourth term is negative. Consequently, there is at least a signal change, and, therefore, $(\varphi_2, 0, 0)$ is unstable.

The synchronous state $(\varphi_1, 0, 0)$ has a positive cosine, consequently, the conditions for its asymptotical stability are $3 - K > 0$ and $3 - K - KG\sqrt{1-(\Omega/KG)^2} > 0$. With these conditions, the lock-in range for a third-order PLL is

(i) $1 \leq K < 3$;

(ii) $G > \Omega/K$;

(iii) $G < \sqrt{9/K^2 - 6/K + 1 + \Omega^2/K^2}$.

Then there is only one synchronous state, $(\varphi_1, 0, 0)$ and the lock-in range results from two bifurcations: a saddle-node, related to the existence of the synchronous state, and Hopf, related to the stability of the synchronous state [8].

The condition $G = \Omega/K$ represents a saddle-node bifurcation, whose diagram is shown in Figure 3.1. Below the surface, there is no synchronous state, and on it the state is non-hyperbolic. Above the surface, there are two equilibrium points: $(\varphi_1, 0, 0)$ and $(\varphi_2, 0, 0)$, so that $\sin\varphi_1 = \sin\varphi_2 = \Omega/KG$ and $\cos\varphi_1 = -\cos\varphi_2 = \sqrt{1-(\Omega/KG)^2}$.

Condition $G = \sqrt{9/K^2 - 6/K + 1 + \Omega^2/K^2}$ represents a Hopf bifurcation, as shown in Figure 3.2. Below the surface, the state $(\varphi_1, 0, 0)$ is asymptotically stable, and above it, unstable.

4. OWMS and TWMS networks

In OWMS topology, the transmission of time signals follows only one direction. The master node has its own time basis that is independent of the other nodes. The time basis of all slave nodes depends on only one node, which can be the master or another slave. OWMS networks can be implemented in two topologies [10], single chain and single star.

TWMS networks have reference signals sent in the two ways of the network. The master has its own time basis, but the time basis of each slave depends on more than one node.

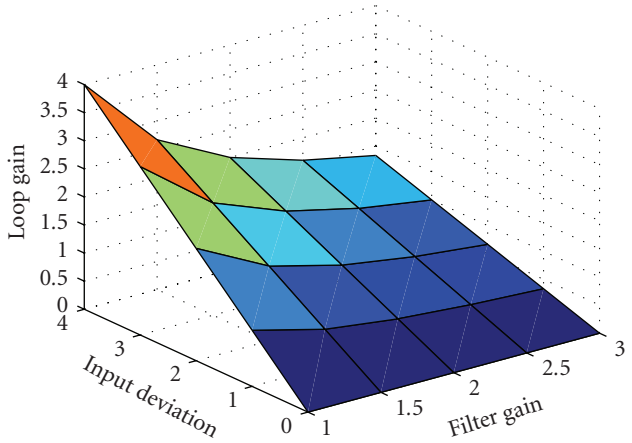


Figure 3.1. Saddle-node bifurcation.

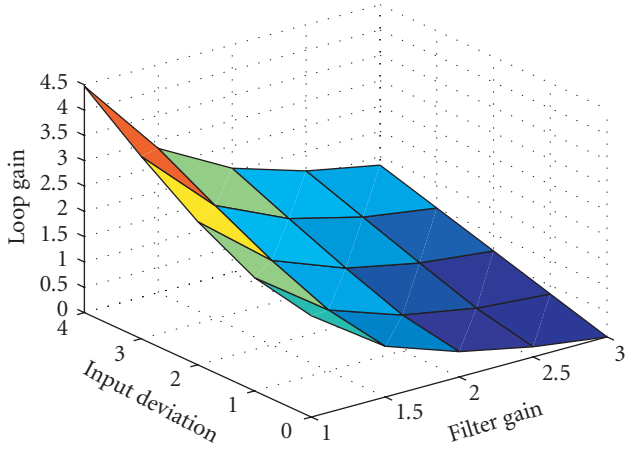


Figure 3.2. Hopf bifurcation.

They can be implemented in four topologies: double chain, double star, single loop, and double loop [10].

Here, only the single and double chains are studied because they are the most common architectures in commercial networks. The single chain topology is composed of a master node, which has an independent time basis, connected to slave nodes in a sequential way, as shown in Figure 4.1. Each slave is a third-order PLL with phase controlled by the node that precedes it in the chain.

The double chain topology is similar to the single chain, but the reference signal, which will be the input of a slave node n, considers the signals from nodes $n-1$ and $n+1$, as shown in Figure 4.2.

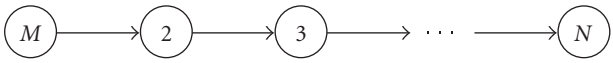


Figure 4.1. Single-chain topology.

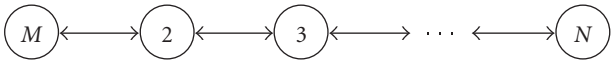


Figure 4.2. Double-chain topology.

In this topology, the time basis of the master node, called node 1, does not depend on the other nodes and is given by a precise and reliable oscillator whose phase is:

$$\phi_M = \omega t + \psi(t), \tag{4.1}$$

where ω represents the frequency of normal operation of master clock and $\psi(t)$ is a perturbation term.

As delays in the main commercial networks are small related to the time constants of the node filters, they are not considered. Consequently, the signal sent by the master to the first slave considers its own phase and the phase of the first slave. Then, the phase of the control signal sent for the first slave is given by the following equation:

$$\Phi_1(t) = 2\Phi_M(t) - \Phi_2(t), \tag{4.2}$$

where $\Phi_2(t)$ represents the phase of node 2, the first slave node.

For this node, the input phase is

$$\Phi_i^{(2)}(t) = \Phi_M(t) - 0.5\Phi_2(t) + 0.5\Phi_3(t). \tag{4.3}$$

From (4.2) and (4.3),

$$\Phi_i^{(2)}(t) = 0.5\Phi_1(t) + 0.5\Phi_3(t). \tag{4.4}$$

As can be seen in (4.4), the input phase of the n-slave node depends on the phase of the nodes $n-1$ and $n+1$. So, for each slave n of the chain, $n = 2,3,\ldots,N-1$,

$$\Phi_i^{(n)}(t) = 0.5\Phi_{n-1}(t) + 0.5\Phi_{n+1}(t). \tag{4.5}$$

For node N, the last of the chain, the input signal will be the output signal of node $N-1$.

5. Numerical experiments

In order to explore the several aspects of the lock-in range and performance parameters, by using MATLAB-Simulink, single and double chain architectures, as described above,

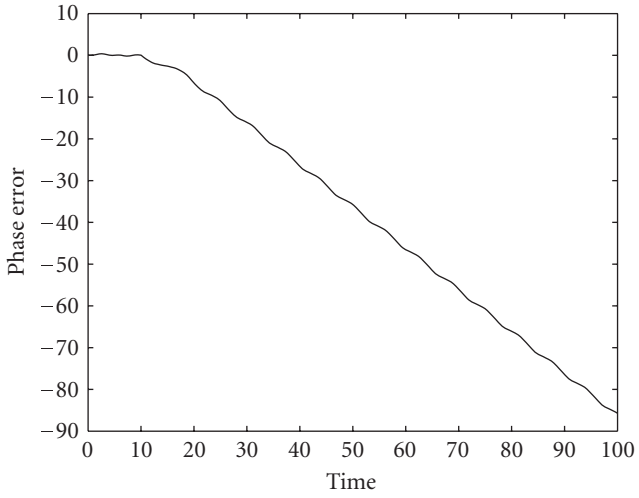


Figure 5.1. Phase error without synchronous state.

were mounted with periodic oscillators as master and built-in PLLs as slaves. Simulations with these architectures were conducted with "Ode-45-Dormand-Prince" [11] with variable step integration method and 10^{-6} of relative tolerance.

The simulations aimed to study the reachability of the synchronous state and to obtain acquisition parameters for the whole network. Input parameters and filter transfer functions were varied trying to confirm the analytical results obtained in Section 3.

The master node was simulated by a periodic signal generator, and a phase ramp starting at tenth second of simulation was added to the master phase in order to analyze the networks capacity in accommodating this perturbation. The input deviation Ω and the free-running angular frequency ω_M were set in 1 rad/s, and the parameters K and G were varied.

The synchronism is analyzed observing the phase error that must be constant in the synchronous state. Network performance includes the double-frequency jitter as it is not completely eliminated being responsible for the oscillations around the synchronous state.

5.1. OWMS. The chains were mounted according to the single chain topology.

One-slave node chain. For $K = 1$, the lock-in range is analytically given by $G \in (1, \sqrt{5})$.

In the simulations, the synchronous state is reachable for $G \in (1.18, 2.2)$. For $G = 1$, the phase error goes to infinite, as illustrated in Figure 5.1, and for G lower than this value, the behavior is the same.

For values of G in the lock-in range, the phase error presents an equilibrium state with a small oscillation, the double-frequency jitter, around it, as can be seen in Figure 5.2 for $G = 1.2$.

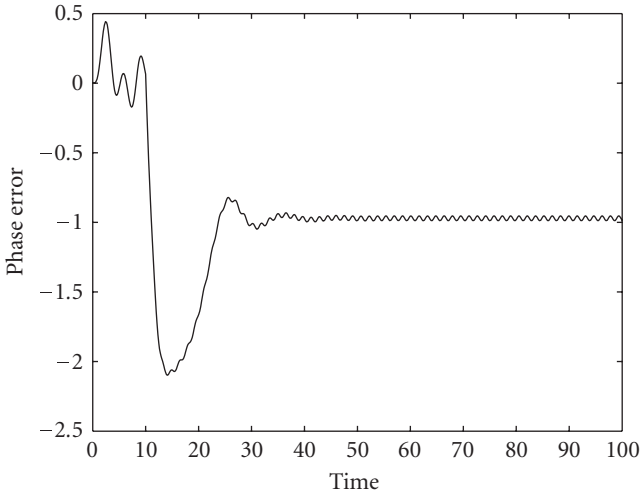


Figure 5.2. Phase error with PLL gain in the lock-in range.

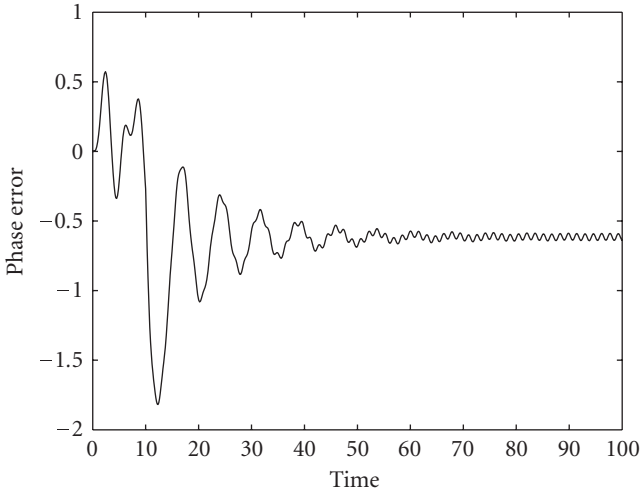


Figure 5.3. Phase error increasing PLL gain in the lock-in range.

When the PLL gain G is increased, the acquisition time and double-frequency jitter increase, as shown in Figure 5.3 for $G = 1.7$.

When the gain value approaches the lock-in range limit ($G = 2.2$), a large amplitude oscillation appears around the synchronous state, as shown in Figure 5.4. With the PLL gain out of this range, there is no synchronous state, as shown in Figure 5.5 for $G = 3.5$.

For $K = 2$, the lock-in range analytically determined is given by $G \in (0.5, \sqrt{2}/2)$.

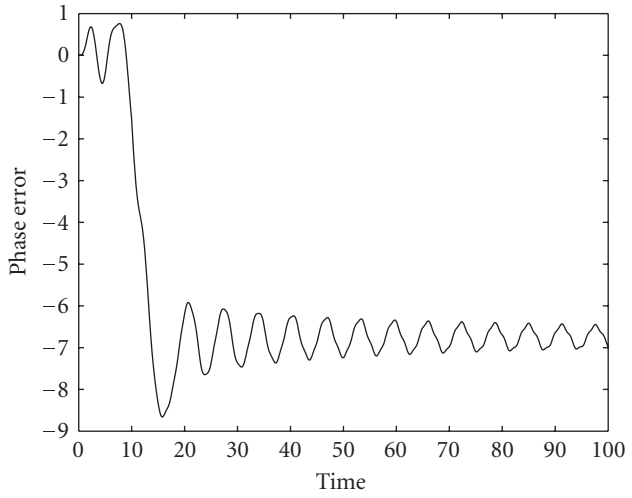


Figure 5.4. Phase error with PLL gain in the lock-in range limit.

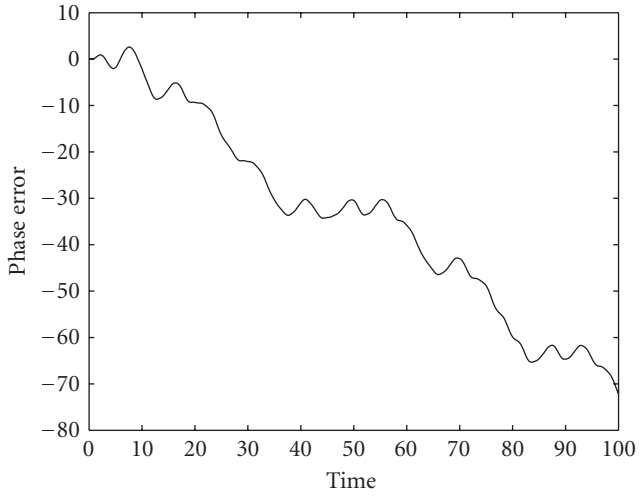


Figure 5.5. Phase error with PLL gain out of lock-in range.

When the simulations are conducted, varying G for the whole theoretical lock-in range, it is experimentally noticed that the synchronous state is not reachable for certain values of G, implying that the practical lock-in range is smaller than the theoretical one. This fact is probably due to nonrobustness of the model in this band of gains.

According to the numerical simulations, the real lock-in range seems to be $[0.5, 0.59) \cup (0.66, \sqrt{2}/2)$. In order to observe this fact, Figure 5.6 shows the result for $G = 0.6$, with the synchronous state not reachable. For $G = 0.67$, reachability is recovered as shown in Figure 5.7.

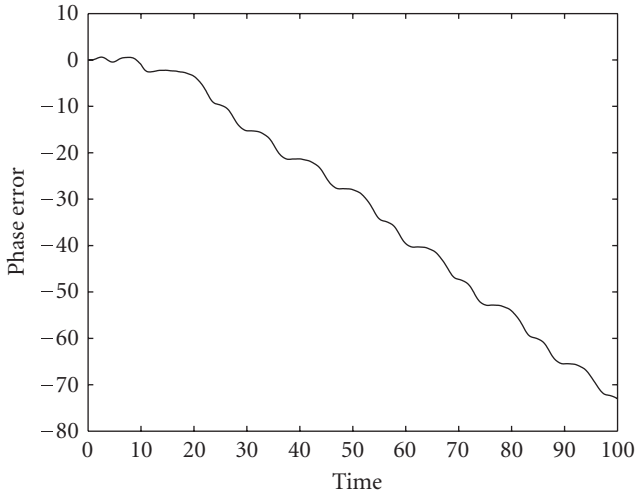


Figure 5.6. Phase error with synchronous state not reachable, but with PLL gain in the theoretical lock-in range.

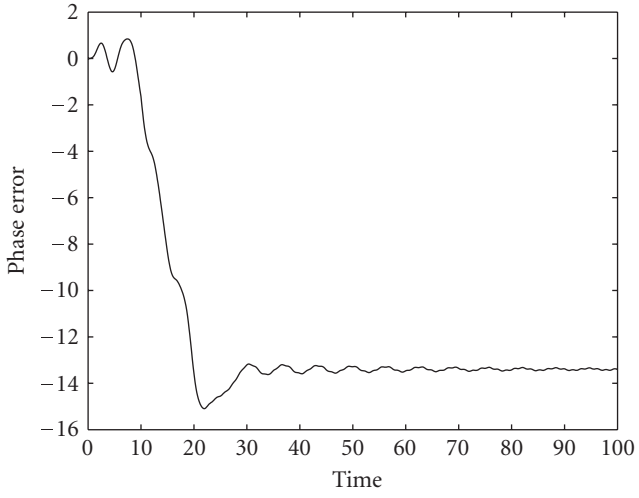


Figure 5.7. Phase error with PLL gain in the lock-in range.

Further experiences show that the higher the parameter K, the smaller the lock-in range. With K next to the limit of the lock-in range ($1 \leq K < 3$), $K = 2.9$, for instance, corresponding to a theoretical range $(0.344, 0.346)$, the synchronous state is not reachable for any G.

The number of slave nodes was increased up to ten gradually and each chain was simulated in accordance with the methodology used in the previous item. It was observed

that to each slave node added to the chain, the synchronizing ranges become smaller, and the settling time increases.

Therefore, the reference signal of the network loses quality while it is transmitted along the chain. Due to this fact, according to G.812 recommendation of ITU-T [12], the higher number of sequential nodes recommended for a single chain is ten, and in the following, results for this type of chain are presented.

Ten-slave node chain. With ten slave nodes, the synchronous state is still reachable, but for a smaller lock-in range, as listed below:

(i) for $K = 1$, the theoretical lock-in range is $G \in (1, \sqrt{5})$. In the simulations, the synchronous state is reachable for $G \in (1.63, 1.64)$;

(ii) for $K = 1.5$, the theoretical lock-in range is $G \in (0.667, 1.2)$, but the synchronous state is reachable for $G \in (0.97, 0.98)$;

(iii) for $K = 2$, the theoretical lock-in range is $G \in (0.5, \sqrt{2}/2)$, and in the simulations, the synchronous state is reachable only for $G = 0.63$ after 400 seconds of simulation;

(iv) for $K = 2.5$, the theoretical lock-in range is $G \in (0.4, 0.447)$, and the synchronous state is reachable for the following gain values: $0.416, 0.436, 0.438, 0.44, 0.443$, and 0.444.

Figure 5.8 shows the phase error for $K = 2.5$ and $G = 0.416$. For the tenth node, the settling-time is high but the double-frequency jitter disappeared, due to the fact that the signal passed through the ten lowpass filters of the chain.

Then, considering the lock-in ranges, the behavior of the whole network with ten slave nodes is satisfactory, showing that the third-order PLL with a Sallen-Key filter for extraction of reference signal in OWMS provides good performance figures.

5.2. TWMS. The analysis of TWMS networks [1] strongly depends on the number of nodes [13], consequently, the simulations follow an increasing sequence of the number of slave nodes.

Two-slave node chain. Running the simulations, the lock-in ranges are the following:

(i) for $K = 1$, the synchronous state is reachable only for $G = 1.3$;

(ii) for $K = 1.5$, the synchronous state is reachable for $G \in (0.8, 0.9)$;

(iii) for $K = 2$, in the simulations, the synchronous state is reachable only for $G = 0.6$;

(iv) for $K = 2.5$, the synchronous state is reachable for $G \in (0.4, 0.5)$, that is, for a lock-in range greater than the theoretical one.

Figure 5.9 shows the phase error in the two slave nodes for $K = 2.5$ and $G = 0.42$. The second node presents a higher settling-time but better double-frequency jitter performance, as expected.

Three-slave node chain. Lock-in ranges are the following:

(i) for $K = 1$ there was no synchronization;

(ii) for $K = 1.5$ the synchronous state is reachable only for $G = 0.7$;

(iii) for $K = 2$, the synchronous state is reachable for $G \in (0.5, 0.6)$;

(iv) for $K = 2.5$, the synchronous state is reachable for $G \in (0.43, 0.48)$, surpassing the theoretical lock-in range again.

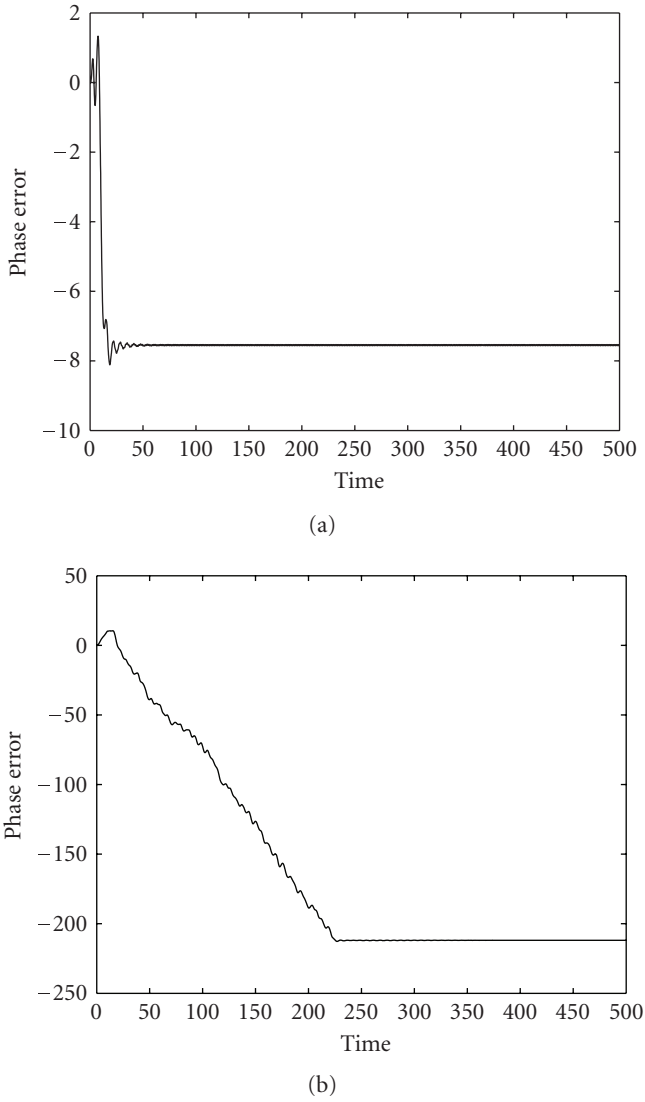


Figure 5.8. Phase error (a) first slave node (b) tenth slave node.

In this case, it is relevant to notice that the settling-time increased and varies from 100 to 250 seconds. Besides, the lock-in range was reduced as listed above.

Four-slave node chain. This chain approached the synchronous state only for $K = 2.5$ and $G = 0.43$, having a considerable oscillation around the synchronous state, as shown in Figure 5.10 for the first and fourth slave nodes. Also it is noticed that a small increase of this oscillation with the increase in the number of slaves. Jitter did not present any significant alteration.

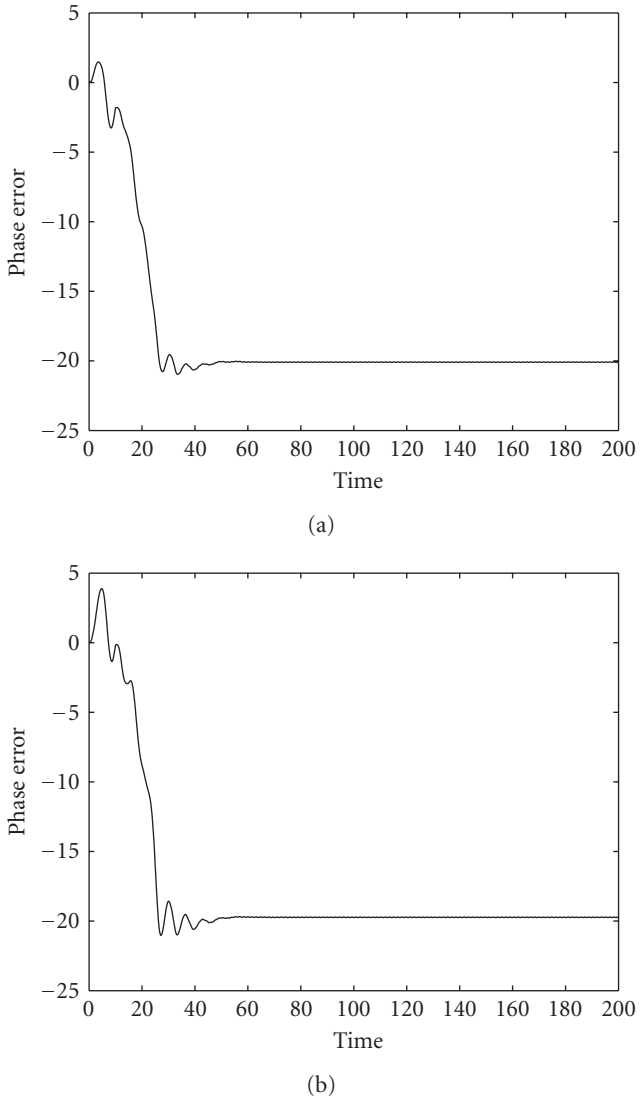
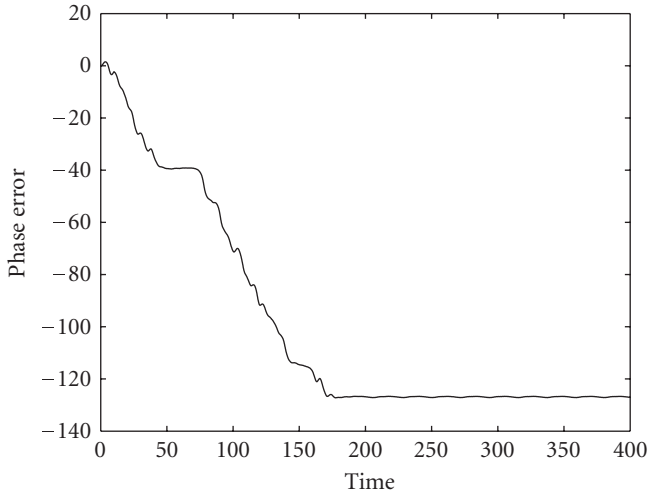


Figure 5.9. Phase error (a) first slave node (b) second slave node.

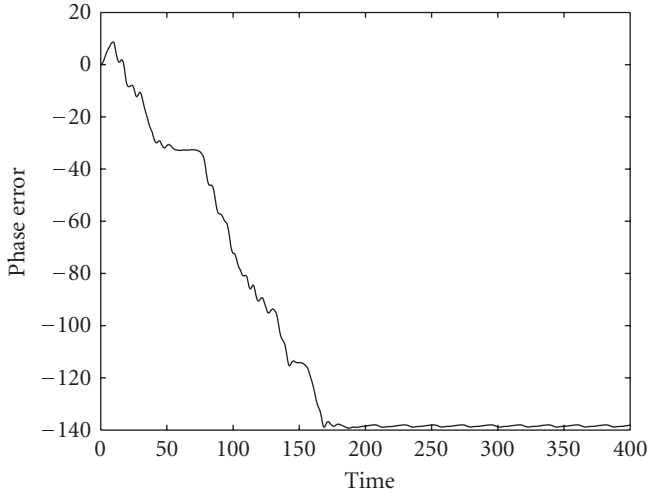
Five-slave node chain. In these conditions, the synchronous state is not reachable. The simulation time was increased to 500 seconds, but for all the values of parameters tested, the phase error went to infinite in all the slaves.

Then it is noticed that the increase in the chain makes the synchronization of TWMS networks difficult considerably, having a limited number of slave nodes, above which the behavior of the network becomes totally unstable.

This result is in accordance to [13] that claims that TWMS networks present limitations in the number of slave nodes that should not be higher than three when a first-order



(a)



(b)

Figure 5.10. Phase error (a) first slave node (b) fourth slave node.

lag filter is used. Simulations have shown that the critical number of slave nodes for third-order PLLs with Sallen-Key filter is four.

6. Conclusions

Third-order PLLs provide satisfactory conditions of synchronism, transient response and double-frequency jitter attenuation when used as slave nodes in MS chain networks. Simulations confirmed analytical results, also showing the reliability of the usual PLL models.

Increasing the number of nodes in a chain makes synchronization more difficult reducing the lock-in range of the OWMS and the TWMS networks. As some theoretical studies show [13], for TWMS chains there is a maximum number of nodes above which the synchronous state is not reachable. This number, when third-order PLLs with Sallen-Key filter are used, is four.

Comparing single-chain (OWMS) with double-chain (TWMS), the OWMS architecture is more indicated for precise clock distribution, since it supports more slave nodes and presents a larger lock-in range.

The limitation in the number of nodes and in the lock-in range for TWMS is the main reason to use this architecture only for process-control in local area networks. In this case, in spite of these problems, transient responses and jitter performance are considerably improved.

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