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Research Article

Optimization of DC-DC Converters via Geometric Programming

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The paper presents a new methodology for optimizing the design of DC-DC converters. The magnitudes that we take into account are efficiency, ripples, bandwidth, and RHP zero placement. We apply a geometric programming approach, because the variables are positives and the constraints can be expressed in a posynomial form. This approach has all the advantages of convex optimization. We apply the proposed methodology to a boost converter. The paper also describes the optimum designs of a buck converter and a synchronous buck converter, and the method can be easily extended to other converters. The last example allows us to compare the efficiency and bandwidth between these optimal-designed topologies.

1. Introduction

Methods of mathematical programming are useful in the processes of design in engineering when these processes have to maximize a certain magnitude and when at the same time there are certain design or operating constraints. The optimal design of DC-DC converters has been studied by several authors. Some of them use graphical methods, but these cannot deal with more than two variables simultaneously, and the variables are rarely constrained. Examples of these methods are the efficiency optimization of a monolithic DC-DC converter [1] and the losses optimization in a switching power converter for envelope tracking in RF amplifiers [2].

The fact that the expressions used are nonlinear has prompted some authors to use nonlinear programming methods, particularly algorithms based on Lagrangian functions. Important related studies are those of Seeman and Sanders [3], who optimized a switched-capacitor converter design by means of Lagrangian functions, and those of Balachandran and Lee [4] and Wu et al. [5], which describe the optimization of DC-DC converters by means

of augmented Lagrangian functions with penalty functions. Other nonlinear programming methods such as the sequential quadratic programming method have also been used for designing of DC-DC converters. For example, Busquets-Monge et al. [6] designed a boost power-factor-corrector converter using this method.

In addition to nonlinear programming techniques, other optimizing methods have been used in converter optimization such as genetic algorithms or probabilistic methods. A genetic algorithm was used to optimize harmonic noise in AC/AC converters in [7], and the Monte Carlo search method has been used to optimize the cost, the weight, and the volume of converters for automotive applications in [8].

Nevertheless, neither general purpose nonlinear programming methods nor the other aforementioned nonlinear optimization techniques ensure that the global optimum is reached because of a local optimum can stop the searching process. Moreover, in some cases, these methods fail to detect the unfeasibility of the problem.

In contrast, unlike other methods that accept any nonlinear function, geometric programming (GP) is able to globally optimize a problem when the objective function and the constraint have a given form. GP ensures that the global solution is readily found or that the unfeasibility is detected very quickly. GP has never been used in the design of DC-DC converters, but it has proved successful in other electrical fields [9–11]. The technique has been used for designing CMOS op-amp [9], electrical transformers [10], and synchronous motors [11].

Although researchers in optimization methods have been interested in GP since the 1960s [12], the real advantages of this technique are only starting to be appreciated now. The reason for this is the significant development of interior point methods for solving convex optimization problems in the last fifteen years [13]. GP methods are now extremely efficient and reliable. GP uses the concepts of monomial function and posynomial function as the form to express objective function and constraints; we review these concepts in the following section.

In the present paper, we apply GP to the task of sizing DC-DC converter components. Specifically, we impose constraints on voltage ripples, current ripples, bandwidth, RHP zero locations, conduction operation mode, and efficiency. First, we choose efficiency as the objective function, then we do the same for the bandwidth. We apply the technique to a boost converter. Also, in subsequent sections, we apply the technique to a buck converter and a synchronous buck converter, then we compare the performances of them to demonstrate the versatility of the procedure.

The paper is organized as follows: we review the GP concepts in Section 2. Section 3 describes the designing magnitudes of a boost converter, the optimization program, and the verification of the solution. Section 4 compares the optimal design of a buck converter with that of a synchronous buck converter. Finally, Section 5 summarizes the main conclusions.

2. Basics on Geometric Programming

The most well-known optimization method is surely the simplex method. This method readily provides a solution to linear programming problems, that is, problems with a linear objective function subject to linear constraints that limit the selection of variable values. On the other hand, general purpose nonlinear optimization methods deliver a

solution for nonlinear problems, but they depend on the starting point, since general purpose nonlinear optimization methods are only able to reach a local optimum. In addition, these optimization methods find it difficult to detect the infeasibility of a problem.

In 1984, Narendra Karmarkar [14] developed an algorithm for linear programming which, in contrast to the simplex method, reaches an optimal solution by traversing the interior of the feasible region. Interior point methods readily solve not only linear optimization problems but also convex problems, that is, problems with a convex objective function and convex constraints. Therefore, any optimization problem that can be modeled as a convex problem can be readily solved by interior point algorithms. There is a great deal of software as MATLAB that has coded interior point methods. We review the concepts of convex set and convex function in the following paragraphs.

A set C is convex if the line segment between any two points in C lies in C; that is, if for any $x_1, x_2 \in C$ and any θ with $0 \leq \theta \leq 1$, we have

$$\theta x_1 + (1-\theta)x_2 \in C. \tag{2.1}$$

Obviously, a generic finite-dimensional real vector space R^n is convex, and a set of R^n with entirely positives coordinates R^n_{++} is also a convex set.

A function $f : R^n \rightarrow R$ is convex if the domain of f is a convex set and if for all points x, y belonging to the domain of f, and given a certain θ with $0 \leq \theta \leq 1$, we have

$$f\big(\theta x + (1-\theta)y\big) \leq f(\theta x) + f\big((1-\theta)y\big). \tag{2.2}$$

Obviously, both linear and affine functions are convex. Another example of convex function is e^{ax} on R, for any $a \in R$. Also, $\sum_{k=1}^{K} e^{a_k^T y + b_k}$ and $\log(\sum_{k=1}^{K} e^{a_k^T y + b_k})$ are convex functions in R^n_{++} [12].

There are certain kinds of nonlinear optimization problems, known as geometric programs, that can be transformed into convex optimization problems by means of a logarithmic change of variables. Such problems can be modeled using the concepts of monomial and posynomial function.

Given a vector $x = (x_1, \ldots, x_n) \in R^n_{++}$, a monomial function is defined as

$$g(x) = c x_1^{a_1} x_2^{a_2} \cdots x_n^{a_n}, \tag{2.3}$$

where c is a positive real constant called the monomial coefficient and $a_1, \ldots, a_n$ are real constants that are referred to as the exponents of the monomial.

The sum of monomial functions is named a posynomial function; that is,

$$f(x) = \sum_{k=1}^{K} c_k x_1^{a_{1k}} x_2^{a_{2k}} \cdots x_n^{a_{nk}}. \tag{2.4}$$

Using these concepts, a geometric program is defined as

$$\begin{aligned} &\text{minimize} && f_0(x) \\ &\text{subject to} && f_i(x) \leq 1 \quad i = 1, \ldots, m, \\ &&& g_j(x) = 1 \quad j = 1, \ldots, p, \end{aligned} \tag{2.5}$$

where $f_0, \ldots, f_m$ are posynomial functions and $g_1, \ldots, g_p$ are monomial functions.

The geometric program (2.5) is not convex; however, it can be made convex by means of the change of variables $y = \log(x)$ or $(x = e^y)$ and replacing $f_i \leq 1$ with $\log(f_i) \leq 0$ and $g_j = 1$ with $\log(g_j) = 0$. Once transformed, the geometric program is written as

$$\begin{aligned} &\text{minimize} && \log(e^y) \\ &\text{subject to} && \log\left(f_i(e^y)\right) \leq 0 \quad i = 1, \ldots, m, \\ &&& \log\left(g_j(e^y)\right) = 0 \quad j = 1, \ldots, p. \end{aligned} \tag{2.6}$$

The geometric program (2.6) can be readily solved using interior point algorithms because it is convex. Thus, modeling an engineering optimization problem as a geometric program solves the problem in a quick and reliable manner. This approach has been used in several engineering problems. In the next section, we analyze design magnitudes in DC-DC converters and confirm that they can be written in posynomial form.

3. Optimal Design in Boost Converters

In this section, we revisit losses, ripples, and other magnitudes that appear in the boost converter design process. On the basis of these expressions, we provide an optimal design and evaluate the influence of converter parameters. Specifically, we optimize the efficiency when the current ripple, voltage ripple, the bandwidth, and the RHP zero location are limited. Afterwards, we optimize the bandwidth when efficiency is constrained.

3.1. The Design Magnitudes in Boost Converters

Although the expressions are well known, we revisit the expressions for the sake of completeness.

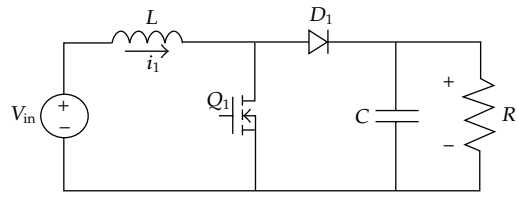

Figure 1: Boost converter.

Figure 1 depicts the boost topology. We consider the following state vector:

$$x = \begin{bmatrix} i_L \\ v_C \end{bmatrix}, \tag{3.1}$$

where i_L is the inductor current and v_C is the output voltage. State equations (3.2) model the converter dynamic behaviour in mode ON (when Q_1 is ON and D_1 is inactive) which corresponds to a value of the control signal $u = 1$, and in mode OFF (when Q_1 is OFF and D_1 is active), which corresponds to $u = 0$. Thus,

$$\begin{aligned} \frac{di_L}{dt} &= \frac{-v_C}{L}(1-u) + \frac{V_i}{L}u, \\ \frac{dv_C}{dt} &= \frac{i_L}{C}(1-u) - \frac{v_C}{RC}, \end{aligned} \tag{3.2}$$

where L, C, and R stand for the inductor value, the capacitor value, and the load value, respectively and V_i represents the input voltage. The expressions of the converter model (3.2) are valid only when it works in continuous conduction mode, as restriction (3.5) imposes.

A consequence of expression (3.2) is that under the hypothesis of low voltage variation in the capacitor, the current ripple is a triangular waveform whose amplitude depends on its slope during T_{ON} and the time that it remains in T_{ON}; namely,

$$\Delta i_L = \frac{V_i d}{L f_s}, \tag{3.3}$$

where V_C is the steady-state output voltage, f_s stands for the switching frequency, and d is the switch duty-cycle which corresponds to $d = T_{ON}/(T_{ON} + T_{OFF})$.

Voltage ripple can be expressed, according to [15], as

$$\Delta v_C = \frac{V_C d}{f_s C R}. \tag{3.4}$$

In addition to ripple constraints, we impose the following restriction to make the boost converter operate in continuous conduction mode (CCM):

$$Lf_s > \frac{V_C}{2I_o} d(1-d)^2. \tag{3.5}$$

Another important property that should satisfy a design is to have a good enough bandwidth. The following expression binds the minimal required bandwidth ω_o:

$$\begin{aligned} \omega_o &= \frac{(1-d)}{\sqrt{LC}}, \\ \omega_o &> 2\pi(af_s), \end{aligned} \tag{3.6}$$

where a is a percentage of the switching frequency.

Given that the boost converter has an RHP zero, we take into account its placement. A design should ensure that the RHP zero location is greater than the crossover frequency; otherwise, the converter will have bad gain and phase margins. The following constraint ensures that the boost converter has good robust margins [16]. This constraint reduces the limitations on dynamical performances caused by the RHP zero

$$\frac{(1-d)^2 R}{L} > 5\frac{(1-d)}{\sqrt{LC}}. \tag{3.7}$$

One of the most important magnitudes in the design of a boost converter is its power consumption, which is made up of conduction losses caused by parasitic resistances, and switching losses caused by parasitic capacitances.

We have used a model of losses that consider only parasitic resistances and capacitances. Nevertheless, parasitic inductances related to layout could be taken into account according to expression of [15], but they are usually much less significant than resistive and capacitive parasitic losses.

In the following analysis, we consider the MOSFET losses, the diode losses, and the ohmic losses in the inductor and the capacitor.

3.1.1. Dissipated Power in the Switches

In this subsection, we first revisit the power losses in the transistor and then those induced by the diode.

The total power consumption of MOSFET P_{Q1} consists of conduction losses P_{ON} and switching losses P_{SW}.

Quantities P_{Q1}, P_{ON}, and P_{SW} can be approximated by

$$P_{Q_1} = P_{\text{ON}} + P_{\text{SW}}, \tag{3.8}$$

where

$$\begin{aligned} P_{\text{ON}} &= \left(\left(\frac{I_o}{(1-d)}\right)^2 + \frac{\Delta i_L^2}{12}\right) D R_{DS}, \\ P_{\text{SW}} &= (V_C - V_f)\left(\frac{I_o}{(1-d)} - \frac{\Delta i_L}{2}\right) T_{\text{swON}} f_s + (V_C - V_f)\left(\frac{I_o}{(1-d)} + \frac{\Delta i_L}{2}\right) T_{\text{swOFF}} f_s, \end{aligned} \tag{3.9}$$

where $I_o/(1-d)$ stands for the MOSFET average current and T_{swON} and T_{swOFF} represent the transition time to on and to off, respectively. Times T_{swON} and T_{swOFF} depend on the gate drive and MOSFET features, R_{DS} stands for the on-resistance of MOSFET, and V_f represents the forward voltage drop in the body diode.

The total power dissipated by the diode P_d can be expressed as

$$P_d = V_f I_o (1-d) + Q_{\text{rr}}^{\text{Schottky}} V_c f_s, \tag{3.10}$$

where $Q_{\text{rr}}^{\text{Schottky}}$ is the reverse recovery charge in the diode. We have considered that the diode is implemented in Schottky technology. For the sake of clarity, we have not taken into account ohmic losses in the diode. Nevertheless, the procedure would allow to consider them adding to expression (3.10) the term $r_d I_{\text{rms}}^2$, where r_d is diode dynamic resistance and I_{rms}^2 is the mean square diode current.

3.1.2. Losses at Passive Elements

The inductor is responsible for a substantial portion of the converter's energy consumption. The losses in this passive element consist of winding losses and core losses, but these can approximately be characterized by a constant equivalent series resistance R_L. Consequently, the power dissipated by the inductive element is expressed as

$$P_{\text{ind}} = \left(\left(\frac{I_o}{(1-d)}\right)^2 + \frac{\Delta i_L^2}{12}\right) R_L. \tag{3.11}$$

Similarly, the capacitor losses can be approximated by

$$P_{\text{cond}} = (I_{\text{eff}_C})^2 R_C, \tag{3.12}$$

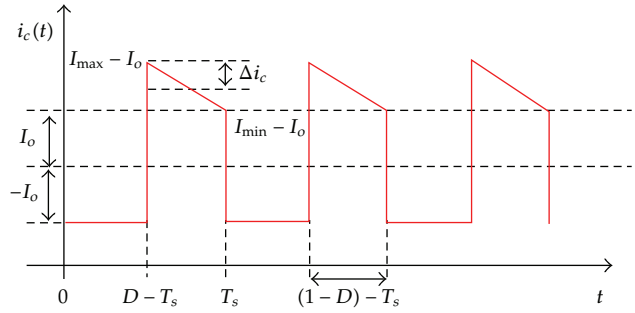

Figure 2: Waveform of the capacitor current.

where R_C is the equivalent series resistance in the capacitive element. The waveform of the capacitor current is shown in Figure 2, and its rms value corresponds to

$$I_{\text{eff}_C} = \int_0^{DT_s} (-I_o)^2 + \int_{DT_s}^{T_s} \left(-\frac{2\Delta i_c}{(1-d)T_s} t + (\Delta i_c - I_o d) \right)^2 dt. \tag{3.13}$$

3.1.3. Total Power Losses and Efficiency in a Boost Converter

Given the expressions (3.1), (3.2), (3.3), and (3.4), the total power losses in the boost converter are written as

$$P_{\text{boost}} = P_{Q_1} + P_d + P_{\text{ind}} + P_{\text{cond}}. \tag{3.14}$$

The terms on the right contribute unevenly depending on the operating conditions of the converter.

Efficiency is defined as

$$\eta = 100 \frac{P_{\text{load}}}{P_{\text{load}} + P_{\text{boost}}}, \tag{3.15}$$

where $P_{\text{load}} = V_C I_o$ is the averaged power at the load.

3.2. Geometric Programming for Boost Converter Optimal Design

In this section, we describe an optimization program that can be solved using geometric programming, because the magnitudes are posynomial. Also, we give an example of the procedure for a realistic set of parameters, and finally, we show that the optimum has been reached. Furthermore, we show the influence of small variations around the optimal point on the performance.

3.2.1. Optimization Program for Boost Converters

In this subsection, we minimize the converter power consumption which is equivalent to maximize the efficiency. Our optimization variables are the size of the storing elements and the switching frequency. In addition, we constrain the ripples, the bandwidth, and the RHP zero location and impose the continuous conduction mode. Thus, the following geometric program allows us to optimally design a boost converter:

$$\begin{aligned}
&\underset{L,C,f_s}{\text{minimize}} \quad P_{\text{boost}} \\
&\text{subject to} \quad L_{\min} \le L \le L_{\max} \\
&\qquad C_{\min} \le C \le C_{\max} \\
&\qquad f_{s\min} \le f_s \le f_{s\max} \\
&\qquad \Delta i_L \le a \ \% \text{ of } I_o \\
&\qquad \Delta v_C \le b \ \% \text{ of } V_C \\
&\qquad \text{CM constraint (3.5)} \\
&\qquad \text{BW constraint (3.6)} \\
&\qquad \text{RHP zero constraint (3.7).}
\end{aligned} \tag{3.16}$$

3.2.2. Example of Optimal Design of a Boost Converter

We show the input values used in the example. The input values are the voltage ratio, the MOSFET and diode parameters, and the variable bounds and the ripple bounds.

The values for the voltage ratio, MOSFET, and diode parameters are shown in Table 1.

Table 2 indicates the bounds imposed on the optimization variables. Some of these limits do not constrain performance; however, others do, and it is particularly important to determine which values these are.

The optimum obtained corresponds to

Optimal values of variables

$$L^* = 79.95\,\mu\text{H}$$

$$C^* = 95.946\,\mu\text{F}$$

$$f_s^* = 104.23\,\text{kHz};$$

Optimal values of objective function

$$P^*_{\text{boost}} = 2.097\,\text{W};$$

Current and voltage ripples and BW

$$\Delta i^*_L = 0.3\,\text{A}$$

$$\Delta v^*_C = 0.1\,\text{V}$$

$$\text{BW}^* = 908.56\,\text{Hz};$$

Efficiency

$$\eta^* = 90.5\%. \tag{3.17}$$

In order to illustrate the versatility of the procedure, next, we show the result when the purpose is to maximize the bandwidth when the efficiency is constrained to be greater than 85%

Optimal values of variables

$$L^* = 10.41\,\mu\text{H}$$

$$C^* = 12.5\,\mu\text{F}$$

$$f^*_s = 800\,\text{kHz};$$

Optimal values of objective function

$$P^*_{\text{boost}} = 2.44\,\text{W};$$

Current and voltage ripples and BW

$$\Delta i^*_L = 0.3\,\text{A}$$

$$\Delta v^*_C = 0.1\,\text{V}$$

$$BW^* = 6.97\,\text{kHz};$$

Efficiency

$$\eta^* = 89.12\%. \tag{3.18}$$

It can be seen that solution (3.2.2) has a much better bandwidth than (3.17) but that this is at the expense of an efficiency decrease.

3.2.3. Verification of the Optimal Solution in a Boost Converter

In this subsection, we analyze some plots to verify the optimality of solution (3.17) and to evaluate which constraint limits the efficiency. The plots indicate that any variation that fulfils

Table 1: Input values of the design example.

V_i	5 V
V_C	10 V
I_o	2 A
R_{DS}	5.2 mΩ
T_{swON}	10^{-8} s
T_{swOFF}	10^{-8} s
Q_{rr}^{db}	$25 \cdot 10^{-8}$ A
$Q_{\text{rr}}^{\text{Schottky}}$	$50 \cdot 10^{-9}$ A
V_f	0.9 V

Table 2: Variable bounds on the design example.

$L_{\text{min}} = 0.1\,\mu$H	$L_{\text{máx}} = 10$ mH
$C_{\text{mín}} = 0.1\,\mu$F	$C_{\text{máx}} = 100\,\mu$F
$f_{\text{smín}} = 10$ kHz	$f_{\text{smáx}} = 800$ kHz
$\Delta I_o < 15\%\ I_o$	$\Delta V_C < 1\%\ V_C$

the constraints around the optimal values (3.16) causes an efficiency decrease. The optimal values of certain variables corresponds to limits of an active restriction, this implies that the relaxation of the limits will increase the efficiency.

Figure 3 depicts the efficiency with respect to frequency values. Red squares correspond to switching frequency values that do not satisfy the current ripple constraint, and black circles are admissible values. The optimal switching frequency value corresponds to the highest black circle. Therefore, the relaxation of the current ripple constraint will increase the efficiency.

Figure 4 depicts the variation of inductance value around the optimum. Red squares represent inductance values that do not comply with the current ripple constraint, and black circles represent the admissible values. The minimum inductance that satisfies the restrictions corresponds to the highest black circle.

We proceed similarly for the capacitor design variable C. The next plot shows that a variation around the optimal capacitor has very little influence on the efficiency (Figure 5).

This graphical process shows that (3.16) is the optimum result and allows us to determine which variables are limited by the design specifications. Finally, the slope of the lines gives an insight into the efficiency increase when a certain constraint is relaxed. Next, we extend this procedure to the buck converter and the synchronous buck converter.

4. A Comparison between Optimal Designs of Buck Converters and Synchronous Buck Converters

The object of this subsection is to show that the proposed procedure can be used to compare different alternatives once we have ensured that they are optimal. Again, we review the magnitudes of the buck and synchronous buck converter (Figure 6). Figure 1 shows these topologies.

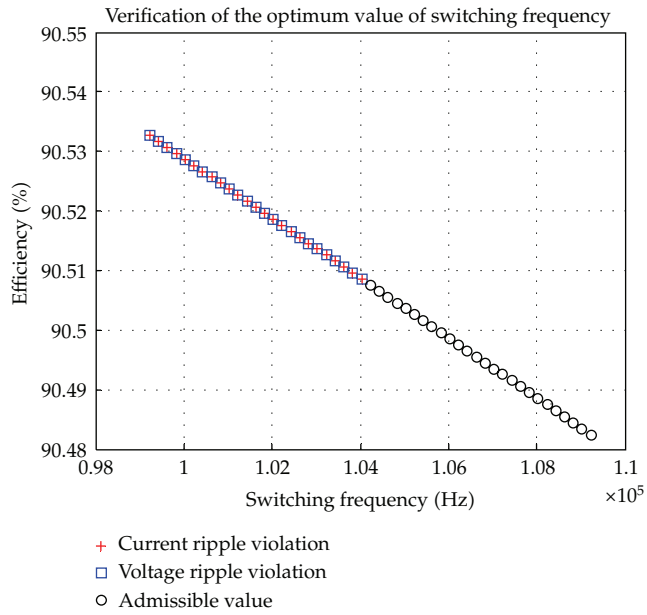

Figure 3: 3-Efficiency versus switching frequency.

4.1. The Design Magnitudes

The state equation corresponds, in both cases, to

$$\begin{aligned} \frac{di_L}{dt} &= \frac{-V_C}{L} + \frac{V_i}{L}u, \\ \frac{dv_C}{dt} &= \frac{i_L}{C} - \frac{V_C}{RC}. \end{aligned} \tag{4.1}$$

Therefore, in the buck and synchronous buck converters, the current and voltage ripples corresponds, respectively, to

$$\Delta i_L = \frac{V_C(1-d)}{Lf_s}, \tag{4.2}$$

$$\Delta v_C = \frac{V_C(1-d)}{8Lf_s{}^2C}. \tag{4.3}$$

The continuous conduction mode constraint is

$$Lf_s > \frac{V_C}{2I_o}(1-d). \tag{4.4}$$

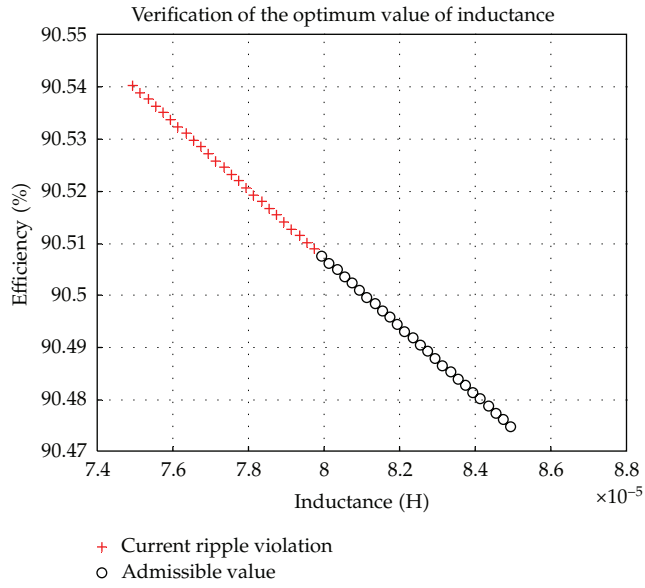

Figure 4: 4-Efficiency versus inductance.

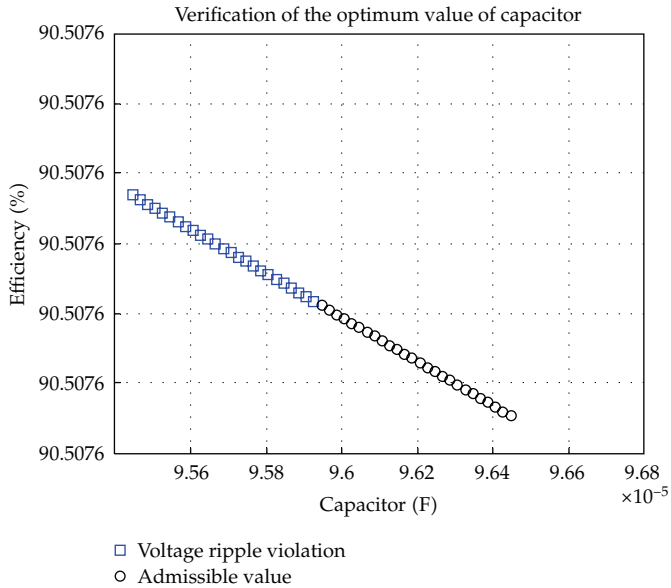

Figure 5: Efficiency versus capacitance.

And the bandwidth can be expressed by

$$\omega_o = \frac{1}{\sqrt{LC}},$$
$$\omega_o > 2\pi\left(10\%\, f_s\right). \tag{4.5}$$

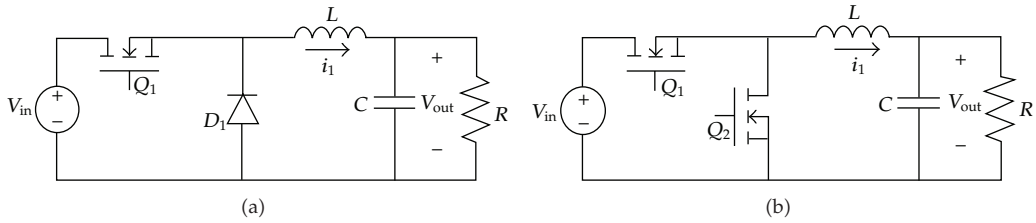

Figure 6: (a) Buck topology (b) Synchronous buck topology.

As in the boost converter, the buck converter's losses occur in the MOSFET, diode, inductor, and capacitor. In the following subsection, we present each of these losses in detail.

4.1.1. Dissipated Power in Buck Converter Switches

MOSFET losses correspond to

$$\begin{aligned} P_{Q_1} &= P_{\mathrm{ON}Q} + P_{\mathrm{SW}}, \\ P_{\mathrm{ON}} &= \left(I_o^2 + \frac{\Delta i_L^2}{12} \right) D R_{DS}, \\ P_{\mathrm{SW}} &= V_i \left(I_o - \frac{\Delta i_L}{2} \right) T_{\mathrm{swON}} f_s + V_i \left(I_o + \frac{\Delta i_L}{2} \right) T_{\mathrm{swOFF}} f_s. \end{aligned} \tag{4.6}$$

And diode losses are described by

$$P_d = V_f I_o (1 - D) + Q_{\mathrm{rr}}^{\mathrm{Schottky}} V_i f_s. \tag{4.7}$$

4.1.2. Losses in Passive Elements

The power dissipated by the inductor is

$$P_{\mathrm{ind}} = \left(I_o^2 + \frac{\Delta i_L^2}{12} \right) R_L. \tag{4.8}$$

Similarly, the capacitor losses can be described by

$$P_{\mathrm{cond}} = \left(\frac{\Delta i_L^2}{12} \right) R_C. \tag{4.9}$$

4.1.3. Total Power Losses and Efficiency in the Buck Converter

Given the expressions (4.6)–(4.9), the total power losses in the buck converter are written as

$$P_{\mathrm{buck}} = P_{Q_1} + P_d + P_{\mathrm{ind}} + P_{\mathrm{cond}}. \tag{4.10}$$

4.1.4. Dissipated Power at Switches in Synchronous Buck Converter

Losses in the high side MOSFET P_{Q1} in synchronous buck converter are the same as P_{Q1} in the buck converter. Losses in the low side MOSFET P_{Q2} corresponds to

$$P_{Q2} = P_{\mathrm{ONQ_2}} + P_{db},$$

$$P_{\mathrm{ONQ_2}} = \left(I_o^2 + \frac{\Delta I^2}{12}\right)(1-D)R_{DS},$$

$$P_{db} = V_f\left(I_o - \frac{\Delta i_1}{2}\right)T_{\mathrm{dead1}}f_s + V_f\left(I_o + \frac{\Delta i_1}{2}\right)T_{\mathrm{dead2}}f_s + Q_{\mathrm{rr}}V_i f_s, \tag{4.11}$$

where V_f represents the forward voltage drop in the body diode, T_{dead1} and T_{dead2} are the dead times introduced by the synchronous rectification, and Q_{rr} corresponds to the body diode charge.

In addition, losses in the storage element are the same in both the buck and synchronous buck converter. Hence, the total power losses in the synchronous buck converter are written as

$$P_{\mathrm{Synchronous\,buck}} = P_{Q_1} + P_{Q_2} + P_{\mathrm{ind}} + P_{\mathrm{cond}}. \tag{4.12}$$

4.2. Optimization Program for Buck Converters and Synchronous Buck Converters

According to expressions (4.10) for the buck converters and (4.12) for the synchronous buck converters, the optimization program is expressed as

$$\begin{aligned}
\underset{L,C,f_s}{\text{minimize}} \quad & P_{\mathrm{buck}} \text{ or } P_{\mathrm{Synchronous\,buck}} \\
\text{subject to} \quad & L_{\min} \le L \le L_{\max} \\
& C_{\min} \le C \le C_{\max} \\
& f_{s\min} \le f_s \le f_{s\max} \\
& \Delta i_L \le a \text{ \% of } I_o \\
& \Delta v_C \le b \text{ \% of } V_C \\
& \text{CCM constraint (4.3)} \\
& \text{BW constraint (4.4).}
\end{aligned} \tag{4.13}$$

In the following section, we instantiate the objective function and the ripple constraints for both converters, and we provide and verify the solution.

4.2.1. Example of Optimal Design

Table 3 shows the input values for the buck converter and for the synchronous buck converter.

The parameters T_{dead1} and T_{dead2} of the synchronous buck converter are equal to 200 ns. The remaining of values are those in Tables 1 and 2.

Thus, the optimal values for each case are

Optimal values of variables	Optimal values of variables
$L^* = 19.34\,\mu\text{H}$	$L^* = 8.23\,\mu\text{H}$
$C^* = 10.98\,\mu\text{F}$	$C^* = 22.05\,\mu\text{F}$
$f_s^* = 86.18\,\text{kHz}$	$f_s^* = 56.68\,\text{kHz}$
Optimal values of objective function	Optimal values of objective function
$P^*_{\text{buck}} = 5.148\,\text{W}$	$P^*_{\text{Synchronous buck}} = 1.542\,\text{W}$
Current and voltage ripples and BW	Current and voltage ripples and BW
$\Delta i_L^* = 1.5\,\text{A}$	$\Delta i_L^* = 2.25\,\text{A}$
$\Delta v_C^* = 0.198\,\text{V}$	$\Delta v_C^* = 0.225\,\text{V}$
$\text{BW}^* = 10.92\,\text{kHz}$	$\text{BW}^* = 11.81\,\text{kHz}$
Efficiency	Efficiency
$\eta^* = 90.66\%$	$\eta^* = 93.57\%$.

(4.14)

As in the boost converter, we try also to optimize the bandwidth when the efficiency greater than 85%. The results are as follows:

Optimal values of variables	Optimal values of variables
$L^* = 2.08\,\mu\text{H}$	$L^* = 0.58\,\mu\text{H}$
$C^* = 0.31\,\mu\text{F}$	$C^* = 1.17\,\mu\text{F}$
$f_s^* = 800\,\text{kHz}$	$f_s^* = 800\,\text{kHz}$
Optimal values of objective function	Optimal values of objective function
$P^*_{\text{buck}} = 6.38\,\text{W}$	$P^*_{\text{Synchronous buck}} = 3.51\,\text{W}$
Current and voltage ripples and BW	Current and voltage ripples and BW
$\Delta i_L^* = 1.5\,\text{A}$	$\Delta i_L^* = 2.25\,\text{A}$
$\Delta v_C^* = 0.75\,\text{V}$	$\Delta v_C^* = 0.3\,\text{V}$
$\text{BW}^* = 197.2\,\text{kHz}$	$\text{BW}^* = 192.5\,\text{kHz}$
Efficiency	Efficiency
$\eta^* = 88.68\%$	$\eta^* = 86.48\%$.

(4.15)

Again, there is a bandwidth increment at the expense of an efficiency decrease.

Table 3: Design example input values.

V_i	10 V
V_C	5 V
I_o	10 A

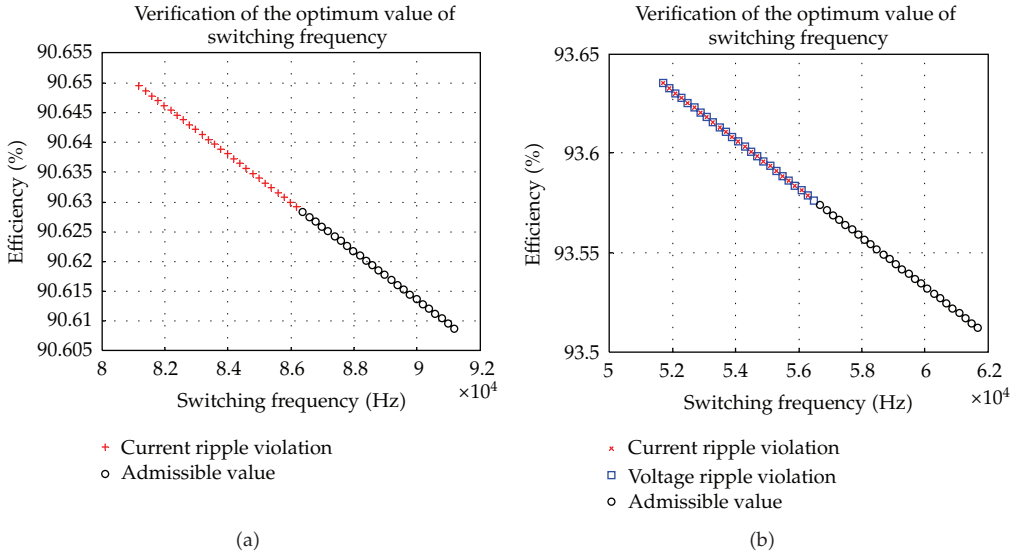

Figure 7: Efficiency versus switching frequency. (a) Buck (b) Synchronous buck.

4.3. *Verification of the Optimal Solution in Buck and Synchronous Buck Converters*

The following plots verify that the optimum (4.14) has been reached and show the sensitivity to optimization variables (Figures 7, 8, 9).

It can be seen that the synchronous buck converter is more efficient than the buck converter and that the size of storing elements differs greatly.

5. Conclusions

The present paper describes a reliable and efficient procedure for optimizing DC-DC converter design that is based on geometric programming. In order to illustrate the procedure, we apply it to a boost converter to show how it optimizes efficiency and bandwidth. Then, we compare optimal designs for a buck converter and a synchronous buck converter, considering both efficiency and bandwidth as optimization functions. We have used plots that show that the optimum has been reached, and they also give an insight into sensitivity to constraint bounds. Proposals to extend the procedure to AC-DC and DC-AC converters are being studied.

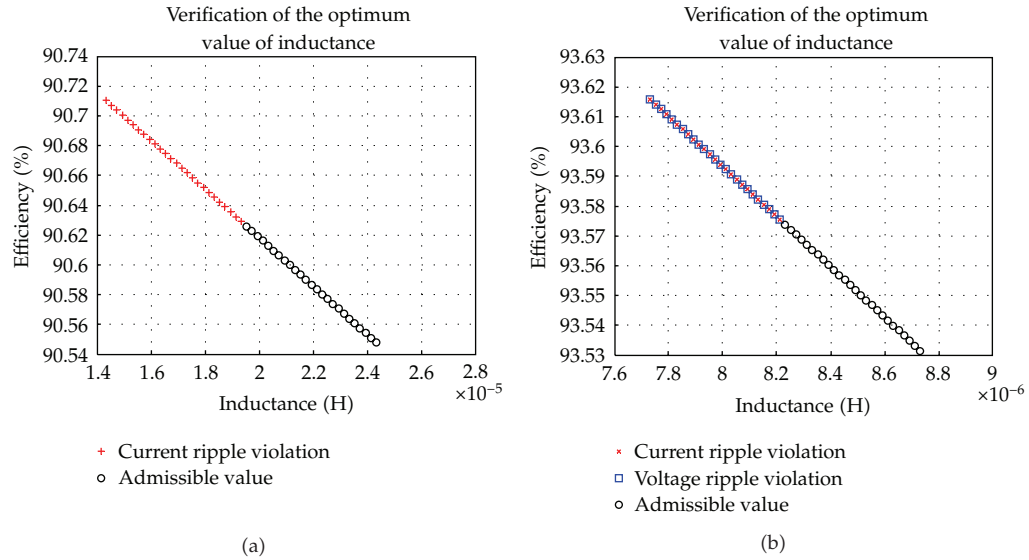

Figure 8: Efficiency versus inductance. (a) Buck (b) synchronous buck.

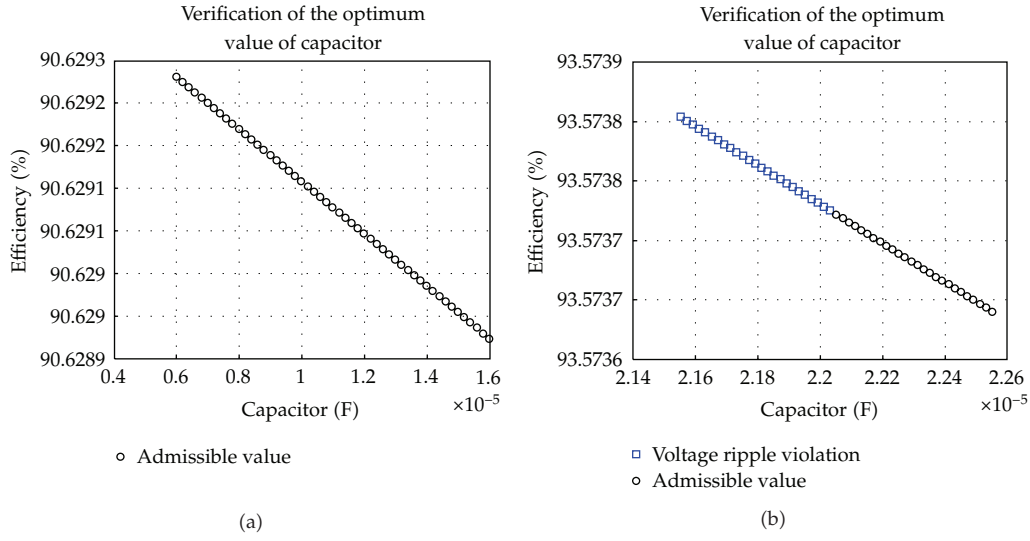

Figure 9: Efficiency versus capacitor value. (a) Buck (b) synchronous buck.

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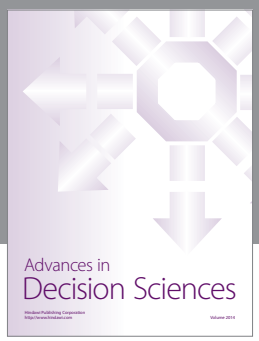

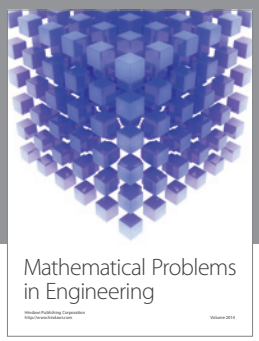

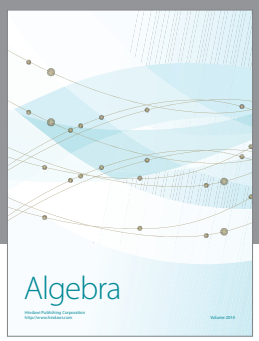

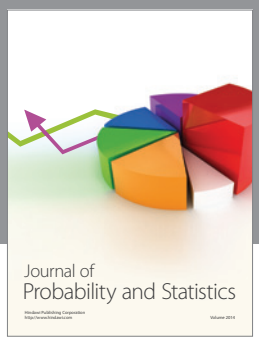

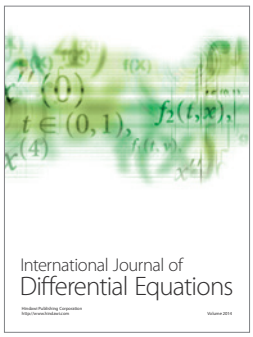

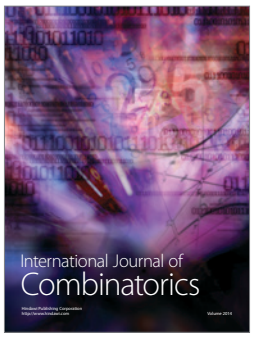

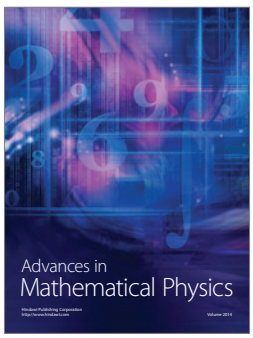

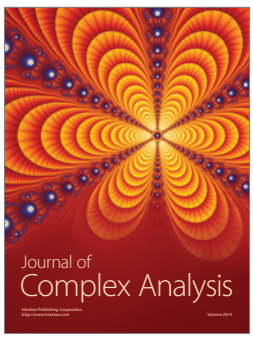

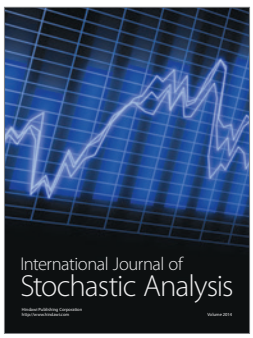

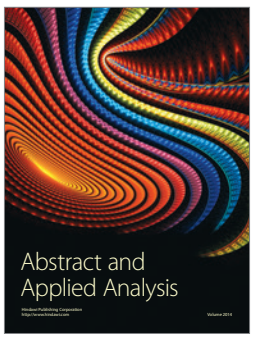

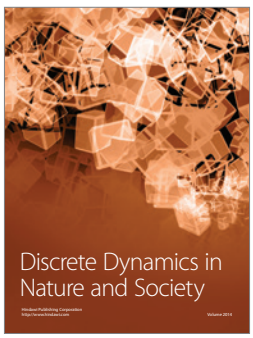

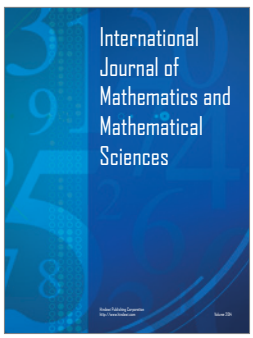

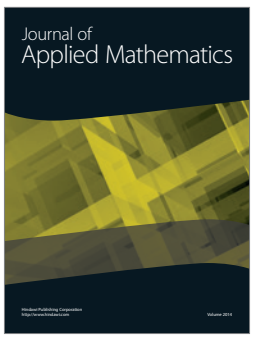

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