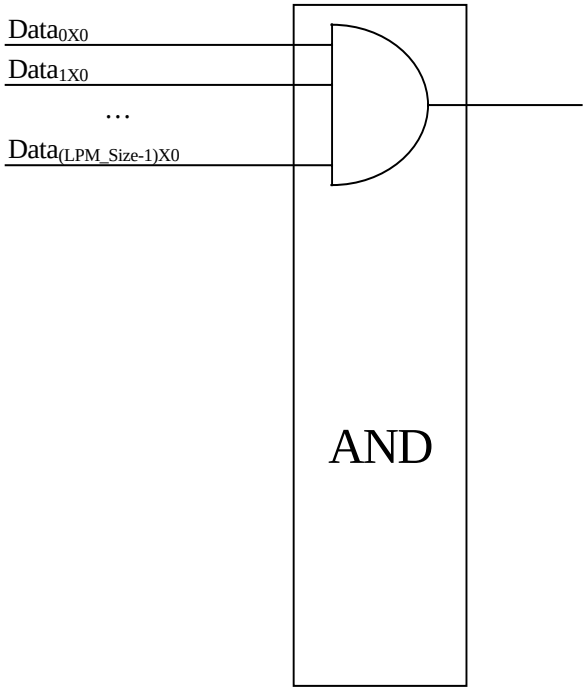
Note that truth table, finite state machine, RAM and ROM modules require more information than can be contained in the LPM netlist to define their function. These modules use supporting files to describe their function. These supporting files use the standard Intel HEX, Berkeley PLA and KISS formats.

1.1.1 Logic Conventions

Where logic equations or logic models are used, the following symbols are used for both

1.2 GATES

1.2.3 LPM_AND

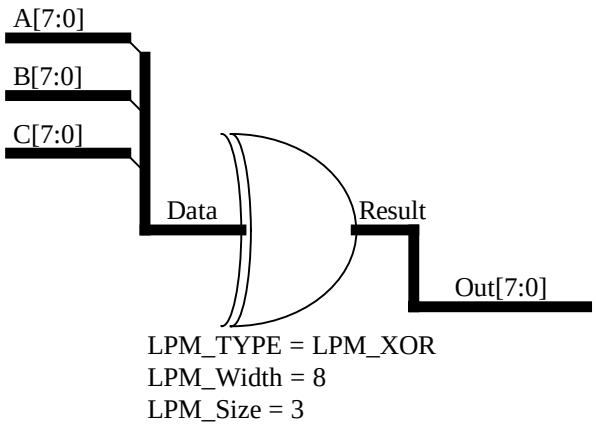


1.2.3.4 Example

1.2.4 LPM_OR

1.2.5.4 Example

Suppose the designers have three 8-bit buses and they want to XOR the corresponding bits of the three buses. This is done using an LPM_XOR with an LPM_Width of 8 and an LPM_Size of three. The LPM_Width of eight indicates that there are eight XOR gates, and the LPM_Size of three indicates that each XOR gate has three inputs.



This diagram is for illustrative purposes only and is not intended to specify any implementation details.

The function performed by the LPM_XOR gate in this case is:

$Out[0] = Result_0 = Data_{2X0} \wedge Data_{1X0} \wedge Data_{0X0} = A[0] \wedge B[0] \wedge C[0]$

$Out[1] = Result_1 = Data_{2X1} \wedge Data_{1X1} \wedge Data_{0X1} = A[1] \wedge B[1] \wedge C[1]$

$Out[2] = Result_2 = Data_{2X2} \wedge Data_{1X2} \wedge Data_{0X2} = A[2] \wedge B[2] \wedge C[2]$

$Out[3] = Result_3 = Data_{2X3} \wedge Data_{1X3} \wedge Data_{0X3} = A[3] \wedge B[3] \wedge C[3]$

$Out[4] = Result_4 = Data_{2X4} \wedge Data_{1X4}$

1.2.6 LPM_BUSTRI

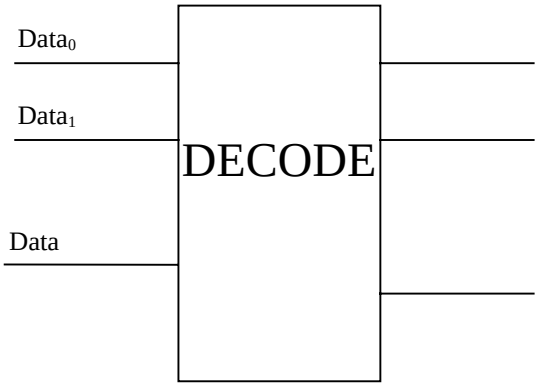
Connection to a Tri-State Bus.

1.2.7 LPM_MUX

1.2.7.4 Example

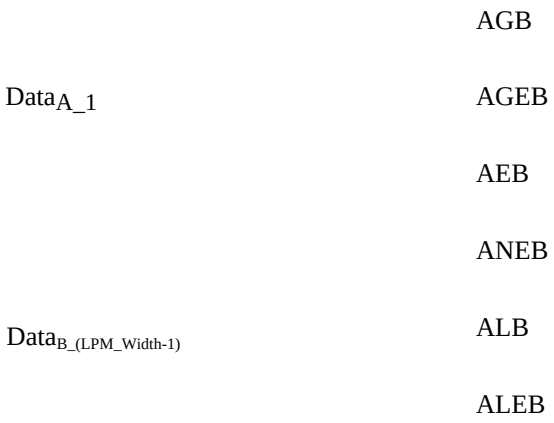
Suppose the designers have three 8-bit buses and they want to select one of the three

1.2.8 LPM_DECODE



1.2.9

1.3.2 LPM_COMPARE



1.3.2.2 Properties

1.3.3

1.3.3.2 Properties

Property	Usage	Value	Comments

1.3.3.4 Example

1.3.4.5

1.3.6

Note 3: **Sset** and **Aset** will set the Flip-flops to the value of LPM_Svalue or LPM_Avalue repectively, if those values are present. If no LPM_Svalue is specified, then **Sset** will set the Flip-flops to all ones, likewise **Aset**.

Note 4: For outputs such as $\mathbf{Q_i}$

1.4.4 LPM_RAM_DQ

1.4.4.3.2 Asynchronous Memory Operations

Totally asynchronous memory operations occur when neither

Note 2: If the **WrClock** port is used, it acts as the clock for write operation and

1.4.5.3 Properties

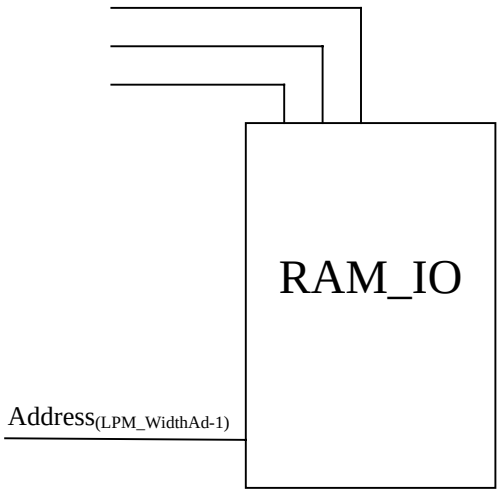
Property	Usage	Value	Comments
LPM_Width	Required	LPM Value > 0	Width of input and output vectors.
LPM_WidthAd	Required	LPM Value > 0	Width of Address Port. Note 1.
LPM_NumWords	Optional	LPM Value > 0	Number of words stored in Memory. Note 2.

1.4.5.4.2 Synchronous Read from memory

RdClock	RdClken	RdEn	Output
X	L	L	No Change
not ↑	H	H	No Change

1.4.6 LPM_RAM_IO

Memory with a single I/O port.



1.4.6.3 Functions

Random Access Memory

Note 1:

Corresponding contents of LPM_ROM:

Address (Hex)	**+0**	**+1**	**+2**	**+3**	**+4**	**+5**	**+6**	**+7**
0	0	0	0	0	0	0	0	0

1.4.8 LPM_FIFO

1.5 TABLE PRIMITIVES

1.5.1 TABLE FORMATS

The full syntax of Truth Table files is defined in section 11.5. A summary is included

3.