# I2C-Master Core Specification

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*Revision History*

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# IO ports

Reset Value: 0x00

The core responds to new commands only when the ‘EN’ bit is set. Pending commands are finished. Clear the ‘EN’ bit only when no transfer is in progress, i.e. after a STOP command, or when the command register has the STO bit set. When halted during a transfer, the core can hang the I2C bus.

### 3.2.3 Transmit register

| Bit # | Access | |
|---|---|---|

### 4.2.4 STOP signal

The master can terminate the communication by generating a STOP signal. A STOP