PWM/Timer/Counter IP Core Specification

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Preliminary Draft

The PTC core has two clock domains. All registers except RPTC_CNTR are in system clock domain.
RPTC_CNTR register can be clocked by either system clock or by external clock reference.

WISHBONE Interface

WISHBONE slave interface connects PTC core to the host system. It is WISHBONE SoC Interconnection specification Rev. B compliant. The implementation implements a 32

PTC Registers

The PTC IP Core has several software accessible registers. The host through these

DAT_I	32	Inputs	Data inputs
DAT_O	32	Outputs	Data outputs