

SRL FIFO Core Specification

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Rev. 0.1
January 22, 2008

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Introduction

The SRL FIFO is a group of First In First Out (FIFO) registers based upon the shift register principle. These are a set of particular at the 64 range of F&+As that have the 8-bit shift register 5-bit outputs known as SRL.

Shift register based FIFOs have been around for years. The definition of shift register based FIFOs is a 64-bit document. Not to surprise when according to work § strFI



Architecture

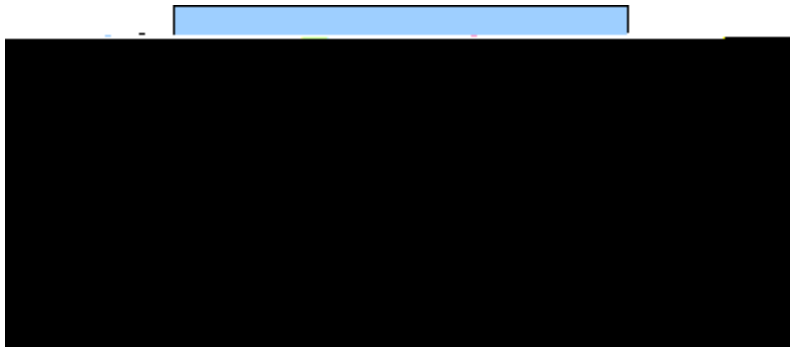


Figure 1: OpenCores Architecture

