TDM controller core

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1 List of authors and changes

2 Project Definition

2.1 Introduction

Time division multiplexing is a scheme used to communicate between systems or devices via shared interface lines. Each device or system

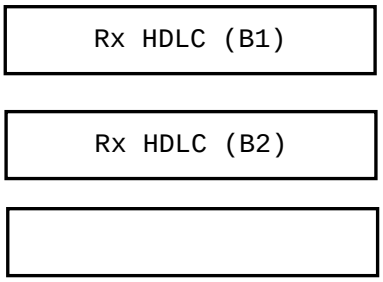
2.2 External Interface

Signal name	Direction	Description
Control interface		
CLK_I	Input	System clock
Rst_n	Input	

Signal Name	Wishbone signal
Master configuration connected to FIFO	Receive channel
CLK_I	CLK_I
Rst	not RST_I
RxD[7:0]	DAT_O(7:0)
RxValid Data	STB_O
RxValid Data	CYC_O

Signal Name	Wishbone signal

□xDone and □x□ y interru□ts are generate when the □x buffer is em□ty and □x buffer has data res□ectively .


Rx HDLC (B1)
Rx HDLC (B2)