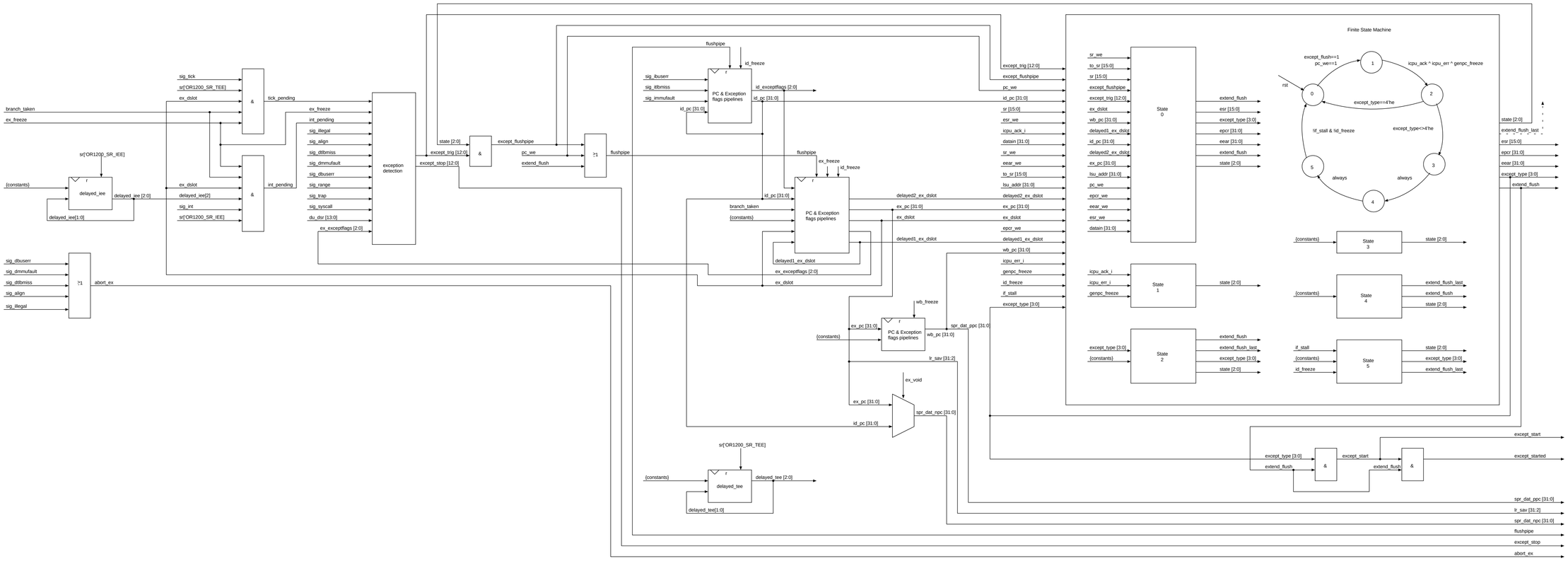
Finite State Machine
sig_tick
sr[OR1200_SR_TEE]
ex_dslot
branch_taken
ex_freeze
&
tick_pending
sr[OR1200_SR_IEE]
{constants}
delayed_iee
delayed_iee [2:0]
delayed_iee[1:0]
ex_dslot
delayed_iee[2]
sig_int
sr[OR1200_SR_IEE]
int_pending
ex_freeze
int_pending
sig_illegal
sig_align
sig_dtlbmiss
sig_dmmufault
sig_dbuserr
sig_range
sig_trap
sig_syscall
du_dsr [13:0]
ex_exceptflags [2:0]
exception detection
except_trig [12:0]
except_stop [12:0]
state [2:0]
&
except_flushpipe
pc_we
extend_flush
≥1
flushpipe
sig_dbuserr
sig_dmmufault
sig_dtlbmiss
sig_align
sig_illegal
≥1
abort_ex
flushpipe
id_freeze
sig_ibuserr
sig_dtlbmiss
sig_immufault
id_pc [31:0]
PC & Exception flags pipelines
id_exceptflags [2:0]
id_pc [31:0]
flushpipe
ex_freeze
id_freeze
id_pc [31:0]
branch_taken
{constants}
PC & Exception flags pipelines
delayed2_ex_dslot
ex_pc [31:0]
ex_dslot
delayed1_ex_dslot
delayed1_ex_dslot
ex_exceptflags [2:0]
ex_dslot
wb_freeze
ex_pc [31:0]
{constants}
PC & Exception flags pipelines
wb_pc [31:0]
spr_dat_ppc [31:0]
lr_sav [31:2]
ex_void
ex_pc [31:0]
id_pc [31:0]
spr_dat_npc [31:0]
except_trig [12:0]
except_flushpipe
pc_we
id_pc [31:0]
sr [15:0]
esr_we
icpu_ack_i
datain [31:0]
sr_we
eear_we
to_sr [15:0]
lsu_addr [31:0]
delayed2_ex_dslot
ex_pc [31:0]
ex_dslot
epcr_we
delayed1_ex_dslot
wb_pc [31:0]
icpu_err_i
genpc_freeze
id_freeze
if_stall
except_type [3:0]
sr_we
to_sr [15:0]
sr [15:0]
except_flushpipe
except_trig [12:0]
ex_dslot
wb_pc [31:0]
delayed1_ex_dslot
id_pc [31:0]
delayed2_ex_dslot
ex_pc [31:0]
lsu_addr [31:0]
pc_we
epcr_we
eear_we
esr_we
datain [31:0]
State 0
extend_flush
esr [15:0]
except_type [3:0]
epcr [31:0]
eear [31:0]
extend_flush
state [2:0]
except_flush==1
pc_we==1
icpu_ack ^ icpu_err ^ genpc_freeze
rst
except_type==4'he
lif_stall & lid_freeze
except_type<>4'he
always
always
icpu_ack_i
icpu_err_i
genpc_freeze
State 1
state [2:0]
except_type [3:0]
{constants}
State 2
extend_flush
extend_flush_last
except_type [3:0]
state [2:0]
{constants}
State 3
state [2:0]
{constants}
State 4
extend_flush_last
extend_flush
state [2:0]
if_stall
{constants}
id_freeze
State 5
state [2:0]
except_type [3:0]
extend_flush_last
state [2:0]
extend_flush_last
esr [15:0]
epcr [31:0]
eear [31:0]
except_type [3:0]
extend_flush
except_start
except_type [3:0]
extend_flush
&
except_start
extend_flush
&
except_started
sr[OR1200_SR_TEE]
{constants}
delayed_tee
delayed_tee [2:0]
delayed_tee[1:0]
spr_dat_ppc [31:0]
lr_sav [31:2]
spr_dat_npc [31:0]
flushpipe
except_stop
abort_ex