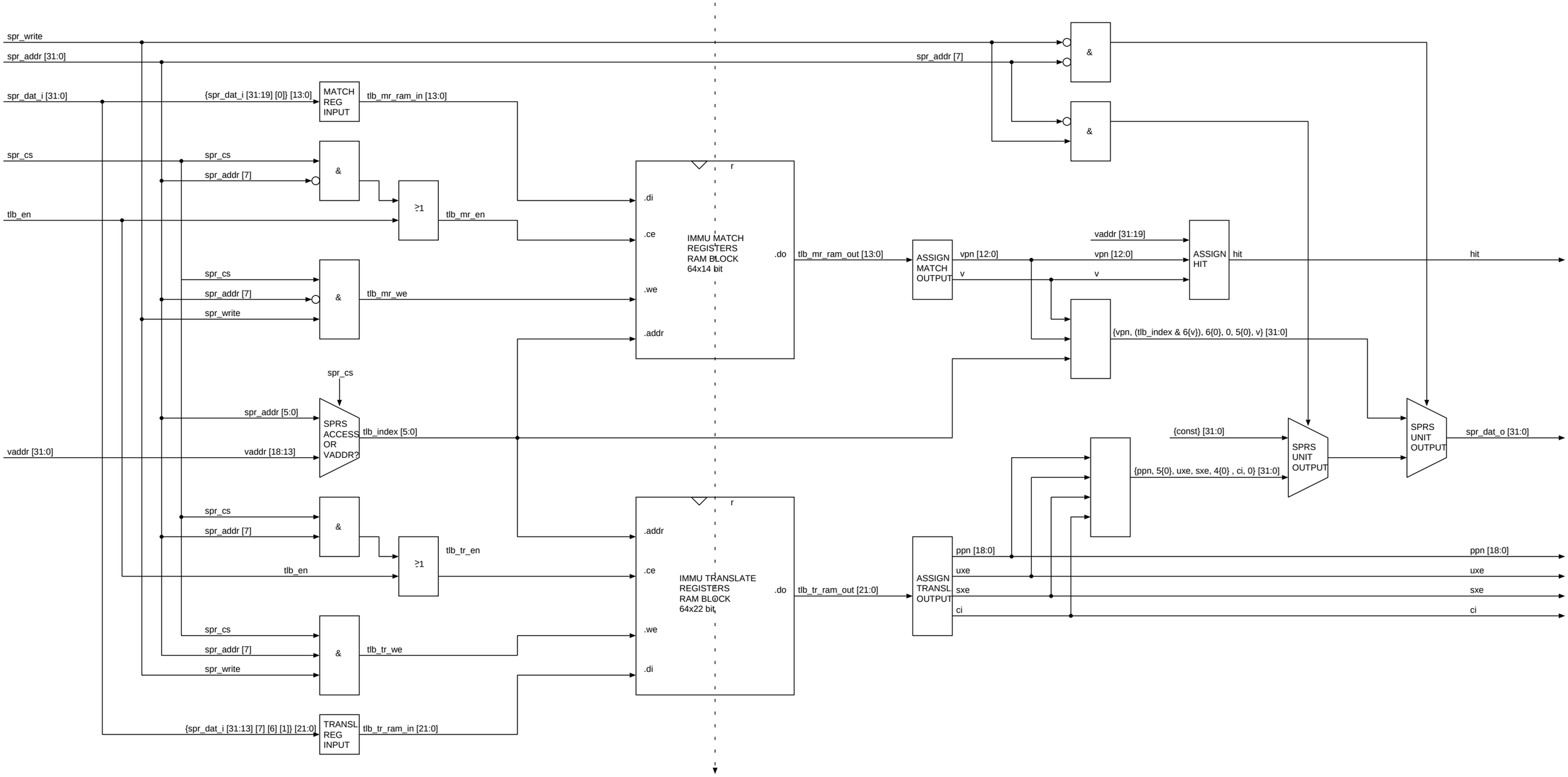
spr_write
spr_addr [31:0]
spr_addr [7]
spr_dat_i [31:0]
{spr_dat_i [31:19] [0]} [13:0]
MATCH REG INPUT
tlb_mr_ram_in [13:0]
spr_cs
spr_addr [7]
&
≥1
tlb_mr_en
tlb_en
spr_cs
spr_addr [7]
spr_write
&
tlb_mr_we
r
.di
.ce
.we
.addr
IMMU MATCH REGISTERS RAM BLOCK 64x14 bit
.do
tlb_mr_ram_out [13:0]
ASSIGN MATCH OUTPUT
vpn [12:0]
v
vaddr [31:19]
vpn [12:0]
v
ASSIGN HIT
hit
hit
{vpn, (tlb_index & 6{v}), 6{0}, 0, 5{0}, v} [31:0]
spr_cs
spr_addr [5:0]
SPRS ACCESS OR VADDR?
tlb_index [5:0]
vaddr [31:0]
vaddr [18:13]
{const} [31:0]
SPRS UNIT OUTPUT
SPRS UNIT OUTPUT
spr_dat_o [31:0]
{ppn, 5{0}, uxe, sxe, 4{0} , ci, 0} [31:0]
spr_cs
spr_addr [7]
&
≥1
tlb_tr_en
tlb_en
r
.addr
.ce
.we
.di
IMMU TRANSLATE REGISTERS RAM BLOCK 64x22 bit
.do
tlb_tr_ram_out [21:0]
ASSIGN TRANSL OUTPUT
ppn [18:0]
uxe
sxe
ci
ppn [18:0]
uxe
sxe
ci
spr_cs
spr_addr [7]
spr_write
&
tlb_tr_we
{spr_dat_i [31:13] [7] [6] [1]} [21:0]
TRANSL REG INPUT
tlb_tr_ram_in [21:0]