

ADDIU

Add Immediate Unsigned Word

ADDU

Add Unsigned Word

BGEZAL

Branch on Greater than or Equal to Zero And Link

BGTZ

Branch on Greater Than Zero

BREAK

Break Point

31	26	25	6	5	0
SPECIAL 000000	Code			BREAK 001101	

Format : BREAK

Fonction : To cause a Breakpoint exception

Description :

A breakpoint exception occurs, immediately and unconditionally transferring control to the exception handler. The code field is available for use as software parameters, but is retrieved by the exception handler only by loading the contents of the memory word containing the instruction.

Restrictions : None

Exceptions : Breakpoint

Notes : None

COP0

Coprocessor system operation

Format : COP0 cop_fun

Fonction : Execute a coprocessor system function

Description :

The coprocessor instruction defined by the cop_fun field is done by the

J

Jump

J 0 0 0 0 1 0	instr_index
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Format : J target**Fonction** : To branch within the current 256 MB-aligned region**Description** :

This is a PC-region branch (not PC-relative); the effective target address is in the “current” 256 MB-aligned region. The low 28 bits of the target address is the instr_index field shifted left 2 bits. The remaining upper bits are the corresponding bits of the address of the instruction in the delay slot (not the branch itself).

Restrictions : None**Exceptions** : None**Notes** : Forming the branch target address by catenating PC and index bits

LUI

LUI

Load Upper Immediate

LW

Load Word

LWC0

Load Word to Coprocessor System

LWC0 110000	base	cs	offset
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MFHI

Move From HI register

SPECIAL	0	rd	0	MFHI
000000	0000000000		00000	010000

Format : MFHI rd

Fonction : To copy the special purpose HI register to a GPR

Description : rd ← HI

MULTU

Multiply Unsigned Word

OR

SLL

Shift Word Left Logical

31 26 25

SPECIAL 000000	0 00000	rt	rd	sa	SLL 000000
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Format : SLL rd, rt, sa

Fonction : To left-shift a word by a fixed number of bits

Description : $rd \leftarrow rt \ll sa$

The contents of the low-order 32-bit word of GPR rt are shifted left, inserting zeros into the emptied bits; the word result is placed in GPR rd. The bit-shift amount is specified by sa.

Restrictions : None

Exceptions : None

Notes : SLL r0, r0, 0, expressed as NOP, is the assembly idiom used to denote no operation.

SLT

Set On Less Than

SPECIAL 000000	rs	rt	rd	0 00000	SLT 101010
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Format : SLT rd, rs, rt

Fonction

SLTIU

Set on Less Than Immediate Unsigned

SLTIU 001011	rs	rt	immediate
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Format : SLTIU rt, rs, immediate

Fonction : To record the result of an unsigned less-than comparison with a constant

Description : rt

SRA

Shift Word Right Arithmetic

SPECIAL	0	
000000	00000	rt

SW

Store Word

SW

