WISHBONE
Interconnect Matrix
IP Core

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Revision History

Rev.	Date	Author	Description
1.0	10/19/01	Rudolf Usselmann	Internal release
1.1	10/3/2002	RU	Fixed a few minor typos.

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Introduction

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Operation

3.1. Master Interface

Each Master interface consists of a WISHBONE Slave interface and decoding logic.

Figure 2: Master interface

The Master Interface performs simple interface signal steering based on the

"Figure 4: Prioritizing Arbiter" on page 7 illustrates the internal operation of the prioritizing arbiter.

3.4. Register File

The Register File consists of 16 registers of 16 bits each. The register file sits behind slave interface 15.

The Register file is selected when a Master selects Slave Interface 15 and the

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Appendix B