In this document, the terms *LSB* and *MSB,*

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the interrupt status to Mode 0. During reset time, the address and data bus go to a high-impedance state, and all control output signals go to the inactive state. Notice that $\overline{\text{RESET}}$

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```
16    ;        a        low order bits of multiplier
17    ;
```

u

Type of Rotate Shift	A	B	C	D	E	F	L

Rest										DD	FD
Bit											
RES	0	C8	C8	C8	C8	C8	C8	C8	C8	C8	C8

[illegible] IN [illegible] A [illegible] OUT [illegible] n [illegible] A [illegible]

[illegible]

[illegible]
NOP [illegible]

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[illegible]	[illegible]	[illegible]
6	20 (4, 4, 3, 3, 3)	5.00

[illegible] 442EH

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[illegible]	[illegible]
B	000
C	001
D	010
E	011
H	100
L	101
A	111

□□□□□□□□
□□□□’

B	000
C	001

[illegible]

[illegible] [illegible]←—[illegible]

[illegible] [illegible]

[illegible] [illegible]

[illegible]

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[illegible]

[illegible]	[illegible]
B	000
C	001
D	010
E	011
H	100
L	101
A	111

[illegible]

[illegible] SRA (IX+3H) [illegible]

7	6	5	4	3	2	1	0
1	1	0	1	1	1	0	0

SRL (lY+d)	6	23 (4, 4, 3, 5, 4, 3)	5.75

[illegible]

[illegible]

[illegible] 2000H [illegible] 2004H [illegible] BIT 6, (IX+4H) [illegible]

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480	30 ← PC after jump
481	00

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[illegible] 07H [illegible] 03H [illegible] 1000H [illegible]

1000H [illegible] 51H
1001H [illegible] A9H
1002H [illegible] 03H

[illegible] OTIR [illegible]