Open Core Protocol™

Overview

The Open Core Protocol (OCP) delivers the first *openly licensed*, *core-centric protocol* that comprehensively fulfills system-level integration requirements.

The OCP defines a comprehensive, bus-independent, high-performance and configurable interface between IP cores and on-chip communication subsystems.

A designer selects only those signals and features from the palette of OCP configurations needed to fulfill all of an IP core's data, control and test signaling requirements.

Once a core is interfaced via the OCP, a complete description is defined for system integration, enabling *core reuse and test reuse without rework*.

The OCP supports data transfer models ranging from simple request-grant through pipelined request-response to more complex out-of-order operations. Very high transfer performance is supported, yet existing IP cores may be inexpensively adapted.

OCP provides a clear delineation of design responsibility boundaries between core authors and SOC integrators.

Highlights

The OCP promotes IP core reusability and reduces design time, design risk, and manufacturing costs for SOC designs.

The OCP is focused exclusively on the needs of an IP core; nothing about the OCP is bus or application specific.

- Enables the creation of IP cores independently of the architecture and design of targeted applications.
- Unifies *all* inter-core communications
- Optimizes die area by configuring into the OCP only those features needed by the core.
- Timing guidelines assure IP core interoperability:
  - **Level 2 -** highest performance interface timing
  - **Level 1** - conservative timing for effortless core connect
  - **Level 0** - protocol without timing specified (esp. useful for verification and simulation tools)
- Plug and Play facilitated with Developer/Core/Rev IDs
- Delivers a firm boundary around each IP core that can be observed, controlled, and validated, enabling portability and full re-use without rework of an IP core's interface or verification / test suites.

The full Open Core Protocol specification is available at:

http://www.sonicsinc.com

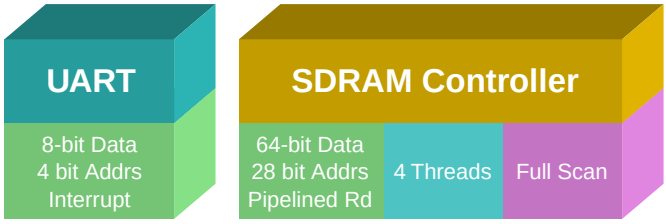
Capabilities

The OCP captures all core characteristics without restricting system arbitration, address map, etc…

- Small set of mandatory signals, with a wide range of optional signals
- Core-specific data and address widths
- Structured method for inclusion of sideband signals: High-level flow control, interrupts, power control, device configuration registers, test modes, etc
- Synchronous uni-directional signaling allows simplified implementation, integration and timing analysis
- Transfers may be *pipelined* for reduced latency
- Optional Burst transfers for higher efficiency
- Multiple concurrent transfer sequences may be managed with *thread identifiers*, for out-of-order completion
- A *connection identifier* may be used to provide end-to-end identification for targets desiring to distinguish initiators for service prioritization, etc.
- OCP is a functional superset of the VSIA's proposed Virtual Component Interface (VCI), adding configurable sideband control signaling and test harness signals.

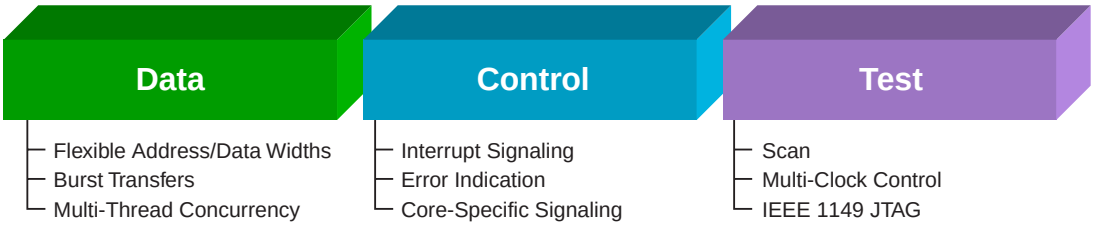
Advantages

- Eliminates the ongoing task of (re)defining interface protocols, then verifying, documenting, supporting them
- OCP readily adapts to support new core capabilities
- Test bench portability simplifies (re-)verification
- Limits test suite modifications for core enhancements
- Any bus structure can be interfaced to the OCP
- Delivers industry standard flexibility and reuse
- Symmetrical signaling enables direct point-to-point communication between 2 cores (without on-chip bus)
- Enables immediate demonstration, evaluation, and integration in an SOC design via Sonics Fast*Forward*™



Very simple through highly complex core signaling can all be handled by this single protocol

Open Core Protocol - OCP



Key Features

Basic OCP

- Master - slave interface with uni-directional signals
- Driven and sampled by the rising edge of the OCP clock
- Fully synchronous, no multi-cycle timing paths
- All signals are strictly point-to-point (except clock & reset)
- Simple request / acknowledge protocol
  - Supports data transfer on every clock cycle
  - Allows master or slave to control transfer rate
- 8/16/32/64-bit data word widths
- 1- through 32-bit address widths
- Pipelined or blocking reads
- Specific description formats for core characteristics, interfaces (signals, timing & configuration), performance

Simple Extensions – enhance Performance

- Burst codes link related transfers into complete transaction
- *Burst transactions* supported:
  - Sequential (defined or undefined length)
  - Streaming (FIFO)
  - Core-specific (cache lines)
- Pipelined (address ahead of data) writes
- Aligned or random byte enables
- Read data flow control

Complex Extensions – enable Concurrency

- *Thread identifiers* enable:
  - Interleaved burst transactions
  - Out-of-order transaction completion
- Thread busy notification prevents interface blocking
- *Connection identifiers* enable:
  - End-to-end system initiator identification
  - Service priority management by system targets

Sideband Extensions – Dedicated Signaling

- Core-specific, user defined signals:
  - System event signals (e.g. interrupts, error notification)
  - Synchronous reset
  - Data transfer coordination (e.g. high-level flow control)

Debug and Test Interface Extensions

- Support structured full or partial scan test environments
- *Scan* pertains to internal scan techniques for a pre-designed hard-core or end user-inserted into a soft-core.
- *Clock Controls* are used for scan testing and debug, including multiple clock domains
- *IEEE 1149* supports cores with a JTAG Test Access Port
- Configurable for JTAG and Enhanced JTAG-based debug for MIPS® (EJTAG), ARM®, TI® DSP, SPARC™ and others

Sonics CoreCreator™

Sonics offers an EDA tool named CoreCreator to automate the tasks of building, simulating, verifying and packaging OCP-compatible cores. CoreCreator also supplies a protocol checker to ensure compliance with the OCP specification. IP core products can be fully componentized by consolidating core models, timing parameters, synthesis scripts, verification suites and test vectors.

SonicsInc
Systems on ICs

Sonics is a venture funded company focused exclusively on SOC design automation products. Sonics' innovative Fast*Forward* SOC Integration System addresses several difficult SOC integration problems. In particular, Fast*Forward* decouples IP cores from each other thereby solving the design, verification, test and IP core reuse problems common to SOC products. Design teams developing consumer, data processing, telecom (wireless or wired), datacom, and mass storage applications gain significant benefits from Sonics solution.

Sonics Inc.

2440 W. El Camino Real, Suite 620
Mountain View, CA 94040
phone: 650 938 2500
fax: 650 938 2577

Europe
Sophia Antipolis Cedex, France
phone: +33 (0)492 94 47 72
fax: +33 (0)492 94 47 73

www.sonicsinc.com

OCP-1999-12-1

Printed in the USA on recycled paper